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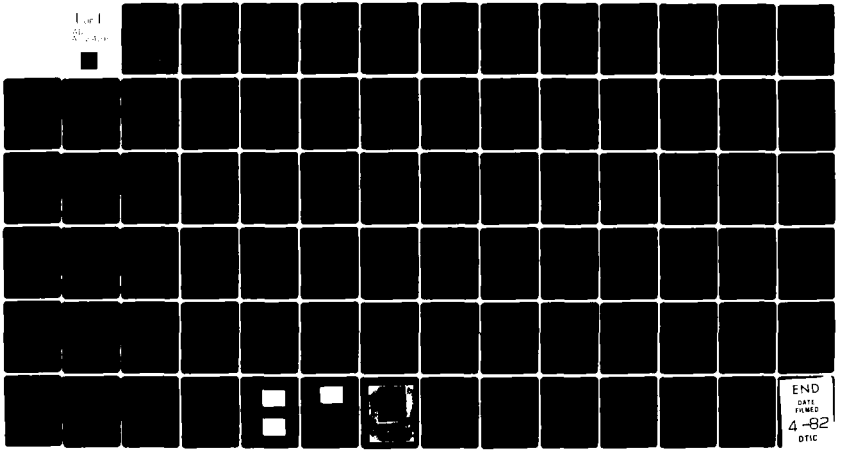

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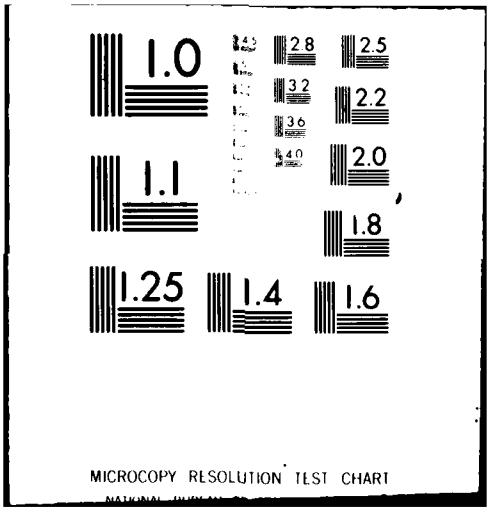
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DNA 5446F

DINS PHOTOPREAMPLIFIER FINAL REPORT

Harris Corporation
Harris Semiconductor
P.O. Box 883
Melbourne, Florida 32901

6 August 1980

Final Report for Period 1 June 1979—6 August 1980

CONTRACT No. DNA 001-78-C-0356

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DEFENSE NUCLEAR AGENCY
Washington, D. C. 20305

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER DNA 5446F	2. GOVT ACCESSION NO. AD-A122	3. RECIPIENT'S CATALOG NUMBER 426
4. TITLE *(and Subtitle)* DINS PHOTOPREAMPLIFIER FINAL REPORT		5. TYPE OF REPORT & PERIOD COVERED Final Report for Period 1 Jun 79—6 Aug 80
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s)		8. CONTRACT OR GRANT NUMBER(s) DNA 001-78-C-0356
9. PERFORMING ORGANIZATION NAME AND ADDRESS Harris Corporation, Harris Semiconductor P.O. Box 883 Melbourne, Florida 32901		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Subtask X99QAXVB205-02
11. CONTROLLING OFFICE NAME AND ADDRESS Director Defense Nuclear Agency Washington, D.C. 20305		12. REPORT DATE 6 August 1980 13. NUMBER OF PAGES 80
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*		15. SECURITY CLASS *(of this report)* UNCLASSIFIED 15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

This work sponsored by the Defense Nuclear Agency under RDT&E RMSS Code B323080464 X99QAXVB20502 H2590D.

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

PhotoPreamplifier	Dielectric Isolated Integrated Circuit
DINS	Rad Hard
Ring Laser Gyro	AR Coatings

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report summarizes the design and development of a radiation-hardened Photodetector circuit using the dielectrically-hardened linear semiconductor process and consisting of a photo diode chip and preamplifier chip. The Photodetector circuit has been developed for use in the Dormant Inertial Navigation System (DINS). The device is a dual detector/amplifier which detects ring laser gyro optical signals (6328A). The report includes

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20. ABSTRACT (Continued)

data derived from functional evaluation, samples of the photodiode and preamplifier stage chips.

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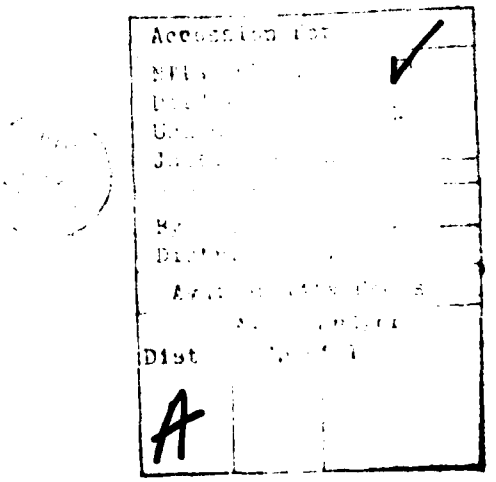

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1.0 INTRODUCTION AND SUMMARY

This report summarizes the design and development of a radiation-hardened photodetector circuit by the Harris Semiconductor Programs Division For the Defense Nuclear Agency under contract number DNA 001-78-C-0356. The photodetector is intended for use in the Dormant Inertial Navigation System (DINS). The device is a dual detector/amplifier which detects ring laser gyro optical signals (6328Å).

The total device consists of two integrated circuit chips. The first chip contains the photodiode detectors and compensating elements as well as the feedback resistors utilized with the input transimpedance amplifier of the second chip. A second gain stage on the amplifier chip then is cascaded to yield a total transimpedance of four (4) meg ohms. With this device a 300 nanowatt signal from the laser is converted to a 500 millvolt output pulse suitable for transmission and drive of a remotely located comparator.

Contained in this report is a design description of the photodiode chip and of the preamplifier chip. In addition to the electrical design and analysis of the devices, the topographical design and fabrication of the devices are described. Finally, the electrical characterization of the amplifier is described. Excellent correlation between the simulated and measured parameters was achieved. A single level mask iteration was required to adjust the amplifier bandwidth and correct a ground hook up error in one channel.

Characterization of the photodiode devices developed under this contract was accomplished by MRC Inc. Results are reported in the report titled: Characterization of the Radiation Hard Harris/DINS Ring Laser Gyro Photodetectors: Contract #DNA-80-C-0140.

Radiation response characteristics of the amplifier section and the total photodetector/amplifier device have yet to be performed. Sufficient devices have been provided under this contract to accomplish this as well as performance characterization at the sytsem level.

2.0 DESIGN REQUIREMENTS

The design requirements of the DINS photo detector system are enumerated as follows:

- The system shall receive a 300 nanowatt, (Min.) 6328Å signal from a ring laser gyro and convert it to a level in the hundreds of millivolts. It must do so in the presence of transient gamma radiation of the specification level and also after the exposure to neutron fluence of the specified level.

- The system shall have an adequate signal-to-noise ratio such that the input signal is not masked by the noise generated during a transient gamma event.

- Assuming the specified photodiode responsivity requirement of .44 Amps/Watt the preamplifier shall have a transimpedance gain of 3 megohms.

- The overall system bandwidth shall be a minimum of 1 megahertz.

- The preamplifier shall be capable of driving a capacitive load (i.e. coaxial cable).

- The preamplifier shall have short-circuit protection.

- A maximum of $\pm$ 20 volts of supply voltage may be used.

- The operating temperature range shall be $-55^{o}C$ to $+125^{o}C$.

3.0 TECHNICAL APPROACH

3.1 Shown in Figure 3,1 is the overall system functional diagram of the DINS photodetector. The system has been divided into two chips, a photodiode chip and an amplifier chip. The photodiode chip also contains four 30K ohm resistors which set the gain of the first stage of amplification. A total of eight chip to chip bond wires shall be required and five bond wires shall be brought out to the package. (Figure 3.2)

3.2 Circuit Partitioning

In order to obtain a 1 to 1 or better signal to noise ratio under minimum drive conditions (300 nanowatts), it is necessary to reduce the noise as much as possible without sacrificing photodiodes during a transient gamma event. Although these photocurrents are applied common mode to the preamplifier by using an identical masked photodiode to the noninverting input, any mismatch in these currents will be applied as a differential signal and therefore show up in the output as the major noise contributor.

Transient I_{pp} (primary photocurrent) is a direct function of the photodiode's total volume since the generation rate $g_E(\ )$ is linear with the depth of the island. However, the input laser signal is exponentially attenuated by the absorption coefficient of the material. Therefore it is the photodiode's area which will directly influence its responsivity. Based on these facts it is evident that the photodiode should have a thin structure with sufficient area for the required responsivity. In this way any mismatch in photocurrents will be minimized by minimizing the total photocurrent.

An island thickness of 2.54 μm was chosen to maintain a small total volume. However this would be incompatible with bipolar transistor fabrication. Therefore the two die approach shown in Figure 3.1 was chosen. The four 30K ohm resistors were chosen to go on the photodiode chip since their fabrication would be more compact using a higher sheet resistivity than the 250 ohm/square of the amplifier chip. A sheet resistivity of 1000 ohm/square will be used for these resistors.

SYSTEM FUNCTIONAL DIAGRAM

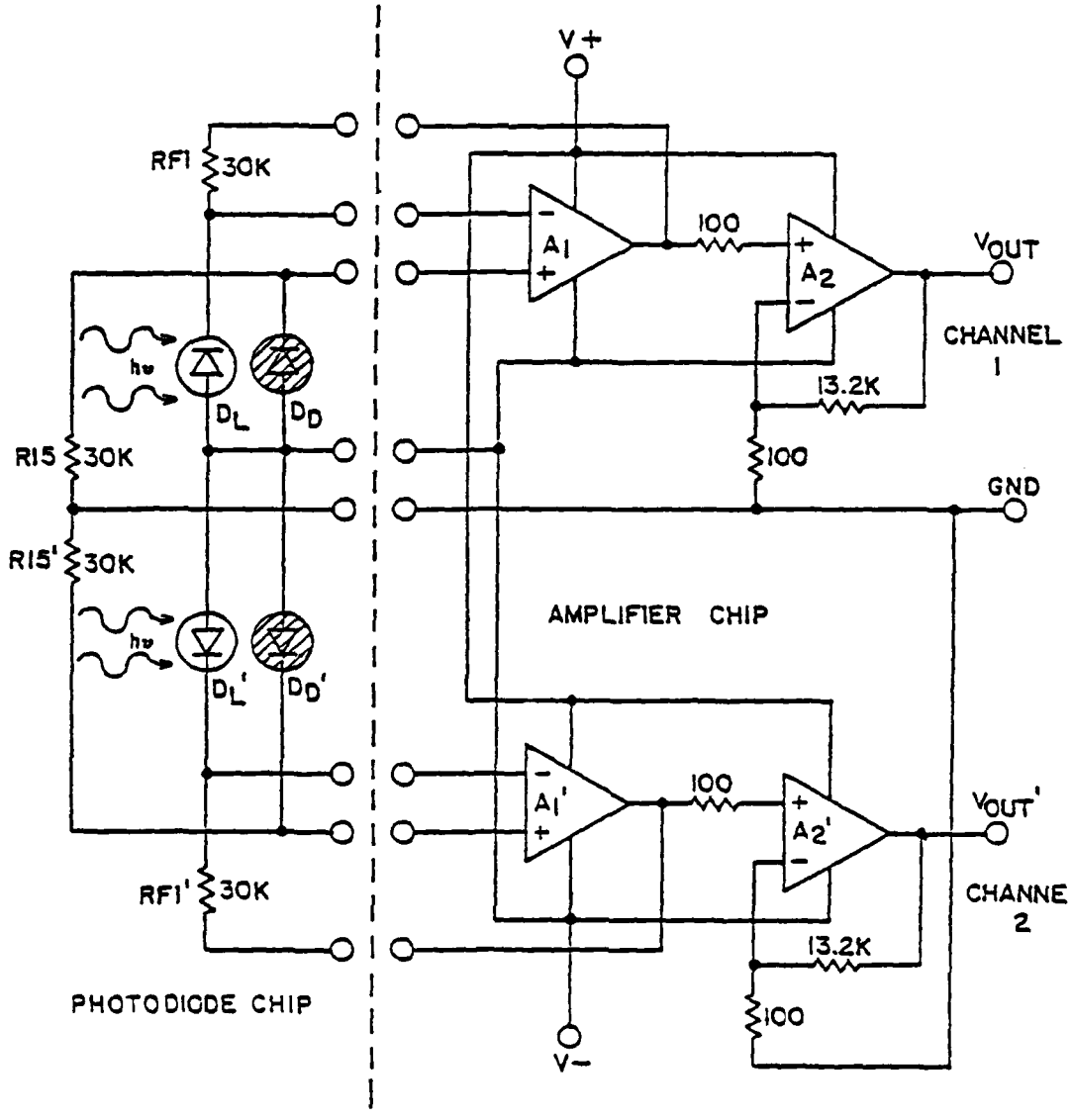


FIGURE 3.1

BONDING REQUIREMENTS

CHIP TO CHIP BOND WIRES

- Channel 1 Stage A, output to resistor RF1
- Channel 2 Stage A′, output to resistor RF1′
- Channel 1 positive input to photodiode D_D and resistor R15
- Channel 2 positive input to photodiode D_D' and resistor R15′
- Channel 1 negative input to photodiode D_L and resistor RF1
- Channel 2 negative input to photodiode D_L' and resistor RF1′
- System ground
- System negative power supply V^-

= 8 Total chip to chip bonds

CHIP TO PACKAGE BOND WIRES

No bond wires are required from the photodiode chip.

From the amplifier chip are required:

- System positive power supply V^+
- System negative power supply V^-
- Output of channel 1 V_{Out}
- Output of channel 2 V_{Out}'

= 5 Total chip to package bonds

FIGURE 3.2

.3 Gain Partitioning

In designing a radiation-hardened preamplifier with an overall gain-andwidth product as large the one required here, it is important that adequate onsideration be given to the distribution of the overall preamplifier gain. he gain of the preamplifier is 3 megohms of transimpedance under worst case emperature and process variability conditions. This worst case criteria also pplies to the specified 1 megahertz bandwidth parameter. Process variability for oth resistors and capacitors is ± 10%. The worst case gain situation will occur t low temperature combined with both low resistors and capacitors. This implies from simulations) that a nominal element, room temperature gain of 4 megohms ill be necessary. Likewise for bandwidth, a nominal figure of 2 megahertz was hosen to guard band against its worst case situation, which will occur at high emperature combined with both high resistors and capacitors.

Achieving a gain-bandwidth product of this magnitude is not feasible ng only a single stage due to stability considerations. Therefore a two ge approach was chosen. Figure 3.3 shows the partitioning. The resistor es are those of the overall circuit. The value of transimpedance of stage (30K) and gain of stage A_2 (133) are values that require realistic gain-dwidth products. Simulations show that under this configuration over 45° phase margin can be obtained from each stage.

A second consideration is the amplifier's worst case input offset con-dition. The output level shift caused by this offset must still allow for the equired maximum output voltage swing, which in this case is about half of a volt.

There are two types of offsets that can be generated at the inputs. Each tage has an inherent voltage offset due to V_{BE} mismatches in each respective in-ut stage. This offset voltage appears at the output amplified by the voltage ain of the stage. In addition, beta degradation and mismatch post-neutron can ause currents (Figure 2) $I_{1(+)}$ and $I_{1(-)}$ to differ by as much as 20%. These urrents which appear across the respective impedances seen at the input ports ill generate an additional offset voltage which is

$$Vos = I_{1(+)} \bullet R15 - I_{1(-)} \bullet RF1$$

The DC voltage gain of transimpedance A_1 is unity. Therefore, this offset voltage appears at the output multiplied by the voltage gain of A_2 which s 133. This same current induced voltage offset will occur at the input of A_2, owever here the impedances seen by the input differential pair is only about 100 hms so the voltage generated across them is small.

NPA betas may fall to 30 and PNP betas to 15 at the specified neutron evel. Therefore:

$\Delta I_1 \bullet RF1 = .44ua \times 30K = 13.2$ mV (current induced offset)

$\Delta I_2 \bullet R31 = 2.4$ ua x 100 = .24 mV (current induced offset)

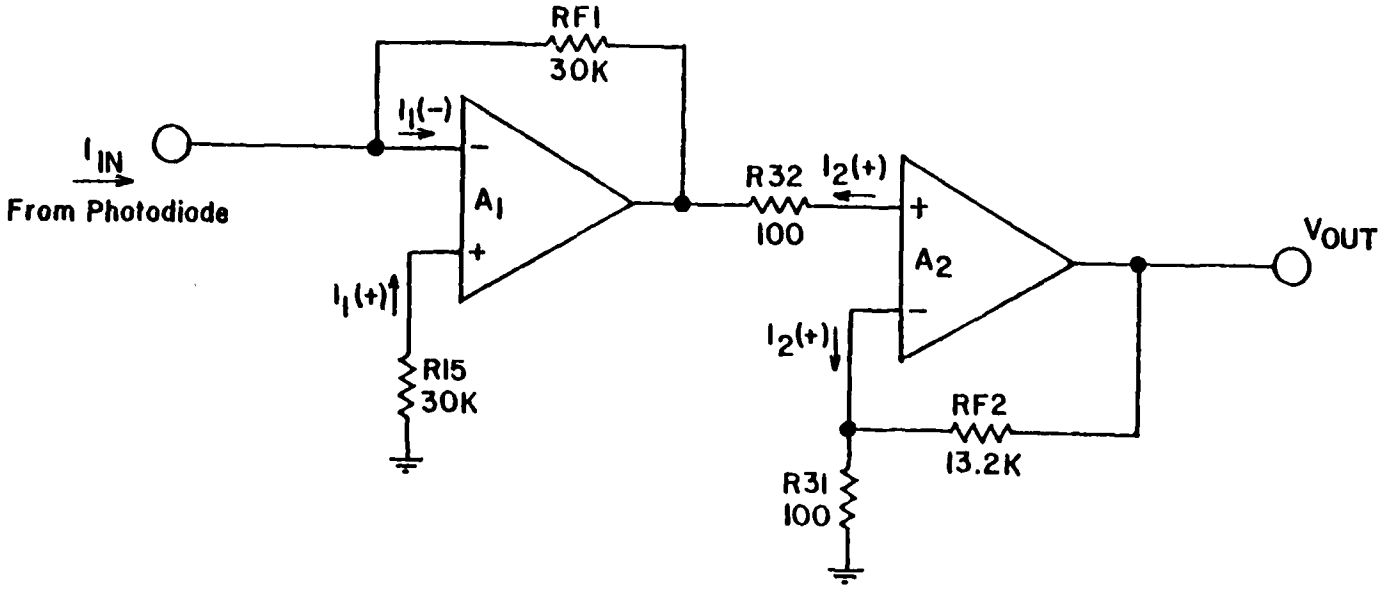
$\Delta V_{IO_1} \leq$ 10 mV

$\Delta V_{IO_2} \leq$ 10 mV

33.4 mV Total V_{IO}

GAIN PARTITIONING

(ONE CHANNEL)



$A_1 = 30K$

$A_2 = 133$

OVERALL GAIN = 4 MEGOHMS

Figure 3.3

The total offset voltage multiplied by the voltage gain of the second stage brings the output voltage to 4.4 volts. Therefore a one half volt swing will not be a problem.

3.4 DIELECTRICALLY ISOLATED P+ - N^- - N+ PHOTODIODE

3.4.1 Theoretical Analysis of Silicon P+ -N^- -N+ Photodiode for 6328Å Laser Detection.

3.4.1.1 Theoretical Analysis of Quantum Yield and Photocurrent:

The theoretical analysis of the photo response for a silicon p+ -n^- - n+ photodiode based on the structure shown in Figure 3.4.1a is presented in this report. The photodiode structure consists of a p+ implanted layer of about 0.15μm thick, and n- layer of 4Ω-cm and 2.5μm thick, and an n+ buried layer of about 2.5um.

The spectral response of the photocurrent and quantum yield for this photodiode is analyzed as follows:

Figure 3.4.1b shows a schematic diagram of the p+ -n^- -n+ photodiode under reverse bias conditions. Let us consider a He-Ne laser (6328Å) impinging on the p+ surface at y = 0. The rate of generation of photocarriers is given by

$$g_E(y) = \phi_o (1-R)\ \alpha e^{\alpha y} \qquad (1)$$

where ϕ is the incident photon flux density, R is the reflection coefficient of silicon.

Under steady state conditions, the total photocurrent density, J_{ph}, produced by the incident photons is the sum of the electron and the hole current components at any cross section of the photodiode, which can be expressed by:

$$J_{ph} = J_n(yo) + J_p(yo) = J_n(yo) + J_p(y1) + J_i \qquad (2)$$

where

$$J_i = J_p(yo) - J_p(y1) \qquad (3)$$

In Eq. (2), $J_n(yo)$ denotes the electron current density at y = yo, $J_p(y1)$ is the hole current density evaluated at y = y1 and J_i is the component of the hole current density arising from the carrier generation in the intrinsic region (i.e., n^- - region). To find the function dependence of the photocurrent and the quantum yield, we need to express $J_n(yo)$, $J_p(y1)$, and J_i as functions of ϕ_o, α, (y_1-y_o), and y_o. Detailed derivation of the photocurrent in each of these three regions (i.e., $0 \le y \le y_o$, $y_o \le y \le y_1$, and $y_1 \le y \le y_2$) have been given by Li and Lindholm [1] for a silicon p-i-n photodiode, which is applicable to the present case. Thus, the photocurrent density for a photodiode shown in Figure 3.4.1b can be expressed by [1]:

$$J_{ph} = q\phi_o (1-R) \left\{ - \frac{1}{\alpha L_n} \left[1-\cosh\left(\frac{y_o}{L_n}\right) e^{-\alpha y_o} \right] \frac{1}{\sinh\left(\frac{y_o}{L_n}\right)} + \frac{e^{-\alpha y_1}}{1+\alpha L_p} \right\} \quad (4)$$

and the quantum yield for the photodiode is given by:

$$\eta = \left| \frac{J_{ph}}{q\phi_o} \right| = (1-R) \left\{ \frac{1}{\alpha L_n \sinh\left(\frac{y_o}{L_p}\right)} \left[1-\cosh\left(\frac{y_o}{L_n}\right) e^{-\alpha y_o} \right] - \frac{e^{-\alpha y_1}}{1+\alpha L_p} \right\} \quad (5)$$

Equation (5) reduces to that of "Gartner's expression" if y_o and R are set equal to zero {2}.

Now we can apply equations (4) and (5) to compute the photocurrent and quantum yield in a p+ -n^- -n+ photodiode shown in Figure 1. The specifications for the photodiode studied in this report are given as follows:

Diode Area: $A_j = 39.3\ \text{Mil}^2 = 2.456\text{x}10^{-4}\ \text{cm}^2$

Junction Depth: (p+ - Layer) $y_o = 0.1\mu\text{m} = 10^{-5}\text{cm}$

Dopant Density: n^- - Layer → $N_D = 10^{15}\ \text{cm}^{-3}, \rho = 4\Omega\text{cm}$

Thickness: n^- - Layer → $y_1 - y_o = 2.5\mu\text{m} = 2.5\text{x}10^{-4}\text{cm}$

Buried Layer (n+ - Layer) Thickness: $y_2 - y_1 = 2.5\mu\text{m} = 2.5\text{x}10^{-4}\text{cm}$

Incident Photon Power Density: Pin = 300nW, $\phi_o = 3.89\text{x}10^{15}\ \text{Photons/cm}^2$

Incident Photon $\lambda_o = 6328\text{Å} = 0.6328\mu\text{m}$

Absorption Coefficient: at λ_o in Si $\Rightarrow \alpha = 3.5\text{x}10^3\ \text{cm}^{-1}$

Hole Diffusion Length in n^- - Region: $L_p \cong 0.01$ cm

Electron Diffusion Length In p+ - Region: $L_n \cong 10^{-3}\text{cm}$

Substituting the above listed numerical values for different parameters in Eqs. (4) and (5) yields:

$$J_{ph} = 0.543 mA/cm^2, \text{ and } \eta = 0.873$$

$$I_{ph} = 1.33 \times 10^{-7} A \text{ for } P_{in} = 300 nw$$

The above results are obtained by assuming that the reflection loss is negligible at the surface of the photodiode.

Table 3.4.1 summarizes the calculated values of photocurrent, quantum yield and responsivity (assuming R = 0) of a silicon p+ - n^- - n+ photodiode for different junction depths (i.e., different thicknesses of the p+ layer) with P_{in} + 300nW.

Table 3.4.1-Theoretical calculations of the photocurrent, quantum yield, and the responsivity of a silicon p+ -n^- - n+ photodiode for different junction depths (y_o). The incident laser beam (6328Å) intensity is assumed equal to 300 nW.

Junction Depth (y_o) μm	Photocurrent I_{ph} (nA)	Quantum Yield (η)	Responsivity (A/W)
0.10	133	0.873	0.44
0.15	132	0.865	0.44
0.20	131	0.856	0.437
0.25	130	0.848	0.433
0.30	128	0.84	0.426
0.40	126	0.825	0.42
0.50	124	0.809	0.413

It is noted that the above calculations are based on the assumptions that the reflection loss is negligible and the dopant densities in both p+ - and n^- - layer are fixed. A change in the dopant density in both p+ - and n^- - layer would in general change the quantum yield as well as responsivity of the photodiode.

3.4.1.2 ANTIREFLECTION (AR) COATINGS

In order to reduce the reflection loss at the silicon photodiode surface, it is important to incorporate the AR coatings in the design of photodiode. Theoretical considerations for the AR coatings in a silicon p+ - n^- - n+ photodiode are described as follows:

1.0. Single Layer AR Coating

To achieve a minimum reflection loss, a single layer dielectric film can be coated on top of the photodiode. Dielectric films commonly used in AR coatings include SiO_2, SiO, Al_2O_3, TiO_2, Ta_2O_5, and Si_3N_4. To obtain minimum reflection loss, the thickness of the dielectric film can be chosen to be equal to quarter wavelength of the incident photon. For examples, if SiO_2 film is chosen, then

with $n_1 = 1.5$ for SiO_2 and $\lambda_o = 6328\text{Å}$, $d_1 = \frac{\lambda_o}{4n_1} = \frac{6328\text{Å}}{4x1.5} = 1055\text{Å}$

If Si_3N_4 is chosen, then with $n_1 = 2.0$, $d_1 = \frac{6328\text{Å}}{4x2} = 781\text{Å}$

The reflection loss can be calculated from

$$R_{min} = \left[\frac{(n_1^2 - n_o n_2)}{(n1^2 + n_o n_2)}\right]^2 \qquad (6)$$

Where n_1 is the index of refraction of the dielectric film, n_o is the index of refraction of air and n_2 is for silicon.

For the case of SiO_2 - Si system the reflection loss is only about 7% when 1100Å SiO_2 is deposited on silicon photodiode. For Si_3N_4 - Si case reflection loss is only 0.016% if 800Å Si_3N_4 AR coating is used!

The above theoretical calculations show clearly that the reflection loss in a silicon photodiode can be reduced to near zero by simply employing a single layer of dielectric film (i.e., SiO_2, or Si_3N_4) as AR coating on the silicon photodiod

2.0. Double Layer AR Coating

In addition to the single layer AR coating, one can also use double layer AR coating. In this case, two different types of dielectric film each with a quarter wavelength thick can be applied to the photodiode surface as AR coating. The minimum reflection loss can be calculated by using the expression:

$$R_{min} = \left(\frac{n_1^2 n_3 - n_2^2 n_o}{n_1^2 n_3 + n_2^2 n_o}\right)^2 \qquad (7)$$

Where n_o is the index of refraction of air, n_1 is the index of refraction for the first AR coating layer and n_2 is for the second coating layer, and n_3 is the index of refraction for the silicon substrate.

If the thickness of SiO_2 and Si_3N_4 AR coatings were chosen to be $\frac{1}{4}$ wavelength of incident Radiation, then the thicknesses of these two layers are given respectively by $d_1 = 1055\text{Å}$ (for SiO_2) and $d_2 = 790\text{Å}$ (for Si_3N_4), and the reflection loss calculated from Eq. (7) is 0.14 which is considerably higher than the single layer AR coatings calculated earlier.

Table 3.4.2 summarizes the calculations of AR coatings for the silicon p+ - n^--n+ photodiode reported here.

Table 3.4.2 - Single layer and double layer AR coatings for silicon $p^+ - n^- - n^+$ photodiode.

Dielectric Film	Thickness α (Å)	Minimum Reflection Loss R_m (at 6328Å)	Refractive Index
SiO_2	1055	7%	1.5
Si_3N_4	781	0.016%	2.0
Ta_2O_5	703	0.3%	2.25
SiO_2/Si_3N_4	1055/781	14%	1.5/2.0

3.4.1.3 SUMMARY

In this discussion, we have shown theoretically that a responsivity of around 0.45 A/W can be achieved by using the proposed geometry and structure in the $p^+ - n^- - n^+$ silicon photodiode. The reflection loss can be minimized to a negligible level if a single layer dielectric film such as SiO_2 or Si_3N_4 with thickness equal to the quarter wavelength of the laser radiation is used as AR coating for the photodiode.

REFERENCES

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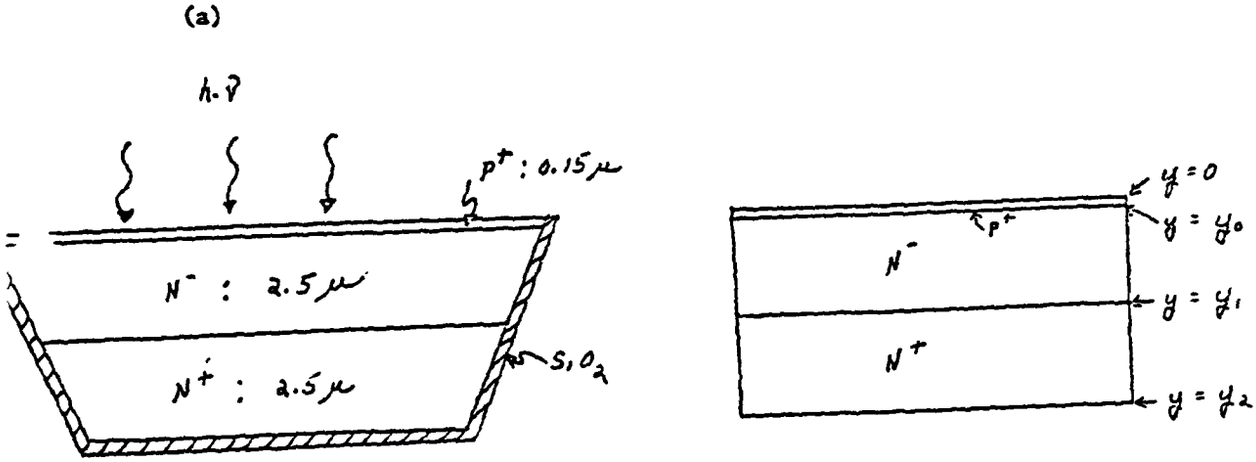
2. W. W. Gartner, Phys. Rev. 116, 84 (1959).



FIGUPE 3.4.1. A SILICON p+ - n⁻ - n+ PHOTODIODE

(i) Reverse Leakage Current (I_R):

The reverse leakage current in the p+ -n^- -n+ photodiode can be calculated from

$$I_R = \frac{q\, n_i\, W_D\, A_j}{2t_i} \qquad (1A)$$

Where n_i is the intrinsic carrier density, W_D is the depletion layer width, A_j is the junction area, and t_i is the carrier lifetime.

For large reverse bias ($V_j \leq -4.2V$), the depletion layer width is given by

$$W_D = W_N = 2.5\mu m$$

If $t_i \geq 100\ ns = 10^{-7}s$, then

$$I_R = \frac{1.6 \times 10^{-19} \times 1.4 \times 10^{10} \times 2.5 \times 10^{-4} \times 2.456 \times 10^{-4}}{2 \times 10^{-7}}$$

$$= 6.877 \times 10^{-10} A \qquad \text{at} \quad 300K$$

(ii) Junction Capacitance of the p+ -n^- -n+ Photodiode

The junction capacitance for the p+ -n^- -n+ photodiode can be calculated from

$$C = \frac{A_j\, C_{jo}}{\left(1 - \frac{V_j}{\phi_b}\right)^{\frac{1}{2}}} \qquad (B1)$$

where

$$A_j = 2.456 \times 10^{-4}\ cm^2$$

$$\phi_B \simeq \left(\frac{2kT}{q}\right) 1_n \left(\frac{N}{n_i}\right) = 0.5756V$$

$$C_{jo} = \left(\frac{q\, \epsilon_s N}{2\phi_B}\right)^{\frac{1}{2}} = 1.2 \times 10^{-8}\ F/cm^2$$

$$C_j = \frac{3.1}{(1-1.75\, V_j)^{\frac{1}{2}}}\ PF \qquad (B2)$$

where v_j is the bias voltage.

For example :

at $V_j = -10V$, $C_j = 0.72pF$.

The capacitance due to SiO_2 isolation around the photodiode can be estimated by

$$C_I \simeq \frac{A_I \varepsilon_{OX}}{t_{ox}} \qquad (B3)$$

where $\varepsilon_{OX} = 4$, $A_I = 2.775 \times 10^{-4}$ cm^2, $t_{ox} = 1.8\mu m$

$$C_I = 0.546pF$$

(iii.) Gamma Radiation Current (I_{pp})

The gamma radiation current can be calculated from the following expression:

$$I_{pp} \cong q g_o A_j (W_p + L) \dot{\gamma} \qquad (C1)$$

where $g_o = 4x10^{13}$/Rad

For the p+ -n$^-$ -n+ photodiode considered, $W_p = W_n = 2.5\mu m$, the effective diffusion length in the buried layer is essentially the thickness of this layer (W_{BL}), thus

$$L \simeq W_{BL} = 2.5\mu m$$

and

$$I_{pp}/\dot{\gamma} = 0.81 \text{ PA/rad/S}$$

If $\dot{\gamma} = 10^7$ Rads/S then

$$I_{pp} = 8.1\mu A$$

3.4.2 Process Description

This section describes the process employed to fabricate the photodiodes. Both the dielectric isolated materials process and the frontside wafer fabrication process will be described as well as the process permutations employed on the first run of photodiodes.

3.4.2.1 Materials Fabrication Process

1.0 Starting Substrate:

Resistivity: 3-5 ohm-cm N-type

Orientation: <1-0-0>

Background Concentration: $\sim 10^{15}$ cm^{-3}

Diameter: 3 - inch

2.0 Buried Layer Formation:

After the buried layer pattern is defined in the field oxide, the buried layer is formed via a two step ion implantation and diffusion operation. The final buried layer process parameters are:

$\rho_s \cong 25$ ohms/sq.

$x_j = 2.5\ \mu$

$C_s \cong 4 \times 10^{19}$ cm^{-3}

3.0 Dielectric Formation:

The dielectric isolation is delineated in the field oxide followed by an anisotropic silicon etch to form the isolation moats. The precise geometry of the moats is defined by the isolation photoresist pattern and the fact that the etch proceeds down the <1-1-1> plane. Following the moat etch, the dielectric oxide is thermally grown.

$t_{ox} = 1.0\ \mu$

4.0 Polycrystalline Silicon Deposition:

The polycrystalline silicon is chemically vapor deposited to achieve the final substrate thickness of $\sim$ 25 mils.

5.0 Final Polish:

The wafers are then chemically-mechanically polished to the specified isolated island thickness of 5 - 7.5 microns.

3.4.2.2 Wafer Fabrication Process

1.0 Initial Oxidation:

The first step in the wafer fabrication process is a thermal oxidation to grow the field oxide followed by a crystal anneal to anneal out the mechanical polish damage.

$t_{ox} = 0.4\ \mu$

2.0 N^+ Cathode Contact:

Following a photoresist operation to delineate diffusion apertures to the n^- cathode, the n+ cathode contact is formed by a two step phosphorus predeposition and diffusion operation. This process results in the following parameters:

ρ_s = 10 ohms/sq.

x_j = 2.5 μ

$C_s = 3.0 \times 10^{20}$ cm^{-3}

3.0 P^+ Anode Contact:

After the P^+ aperture pattern is etched in the field oxide, the P^+ anode contacts are formed with a two step boron predeposition and diffusion process. The resulting parameters are:

ρ_s = 125 ohms/sq.

x_j = 0.6 μ

$C_s = 4.0 \times 10^{19}$ cm^{-3}

4.0 Anode Formation:

A 5 mil radius circular pattern is etched in the field oxide for the anode of the photodiode. Subsequent to the etching operation, 1100Å of thermal oxide is grown in the opened anode area. This oxide serves to control the peak of the anode ion implantation. Boron is then ion-implanted to form the p^+ anode. The following are the ion implantation parameters:

Energy = 100 KeV

Dose = 2.3×10^{-3} coul.

Projected Range = 0.12 μ

Peak Concentration = 2.5×10^{19} cm^{-3}

5.0 Antireflection Coating and Si_3N_4 Passivation:

If a silicon nitride AR coating is desired, then the 1100Å of thermal oxide is removed from the anode area and 800Å of silicon nitride is chemically vapor deposited over the wafer. If an SiO_2 AR coating is preferred, then the 1100Å of thermal oxide is left over the anode and the 800Å of silicon nitride is later etched from the anode area, exposing the 1100Å SiO_2 AR coating.

6.0 Contact Apertures:

The contact aperture pattern is plasma etched in the silicon nitride and the underlying thermal oxide is dipped out creating the anode and cathode contact apertures.

7.0 Interconnect Formation:

A 1.2μ thick aluminum/2% silicon film is sputtered over the wafer and the interconnect pattern is then delineated in this film.

8.0 Passivation and Backlap:

An 8000Å film of SiO_2 is chemically vapor deposited over the wafer to serve as a passivation layer.[2] The bond pad pattern and the anode of the photodiode is etched in the passivation oxide. The wafers are then thinned to the final die thickness of 11 mils.

3.4.2.3 Vertical Cross-Section

Figure 3.4.2 depicts the vertical cross-section of the dielectrically isolated photodiode.

3.4.2.4 Process Permutations

To establish an optimum process for the photodiode fabrication, several process permutations were employed on the 1st run.

1) Buried Layer vs. No Buried Layer:

Wafers 1 - 10: Buried Layer

Wafers 11 - 20: No Buried Layer

2) Antireflection Coating:

Even numbered wafers: Silicon nitride AR

Odd numbered wafers: Silicon Dioxide AR

3) Crystal Anneal:

Anneal #1: Wafers 6-10 and 16-20

Ramped initial oxidation and anneal

Anneal #2: Wafers 1, [illegible], 11 and 12

Harris standard initial oxidation and anneal

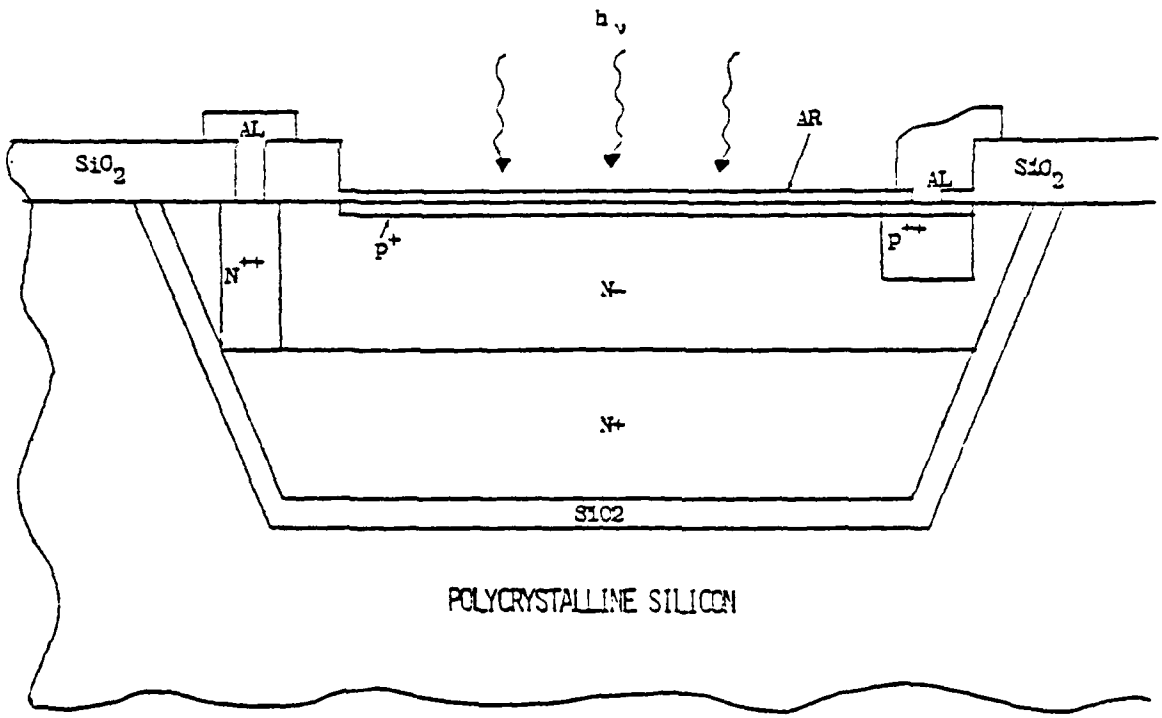
Anneal #3: Wafers 3, 4, 5 and 13, 14 and 15

Harris standard initial oxidation with no anneal

3.4.4.0 Preliminary Results

The responsivity and dark currents with and without radiation and the photocurrent generation constant of the various process permutations were evaluated by Honeywell personnel. This section summarizes the results of those evaluations.

IDEALIZED VERTICAL STRUCTURE
OF PHOTODIODE



N+ Buried Layer

$C_s \simeq 1.0 \times 10^{19}$ cm^{-3}

N+ thickness = 2.5u

N- Layer

$C_B \simeq 1.0 \times 10^{15}$ cm^{-3}

N- Thickness = 2.5u

P+ Anode

C(Peak) $\simeq 2.5 \times 10^{19}$ cm^{-3}

$\overline{R_p}$ = 0.12u

P++ Anode Contact

$C_s \approx 4.0 \times 10^{19}$ cm^{-3}

P++ Penetration = 0.6u

N++ Cathode Contact

$C_s \approx 3.0 \times 10^{20}$ cm^{-3}

N++ Penetration $\simeq$ 2.5u

Figure 3.4.2

PROCESS DESCRIPTION: PHOTODIODE PREAMP

The preamp uses a standard Harris linear process featuring dielectric isolation, complementary NPN/PNP devices, MOS capacitors and implanted high sheet resistors. The process description will be divided into a material fabrication section and a frontside processing section. Material fabrication covers the sequence from starting material to slice grind and polish, frontside processing covers initial oxidation through backlap.

1. MATERIAL FABRICATION. This sequence is outlined below.

Initial Oxidation
P Collector Photoresist and Etch
P Collector Diffusion
N+ Buried Layer Photoresist and Etch
N+ Buried Layer Diffusion
Isolation Photoresist and Etch
Anisotropic Moat Etch
Isolation Oxidation
Polycrystalline Si Deposition
Front Side Lap and Polish

- Initial oxidation grows a masking oxide on the polished slice. Starting resistivity is 3-6 ohm-cm; orientation is 1-0-0; slide diameter is 3"; and slice thickness is 20 mils.

- P collector photoresist/etch defines collector areas for PNP devices.

- P collector diffusion establishes a deep, lightly doped boron diffusion for use as a PNP collector. (Figure 3.5.1).

- N+ buried layer PR and diffusion establishes a heavily As doped layer used as a low resistivity subcollector for the NPN devices. (Figure 3.5.2)

- Isolation photoresist defines the isolation grooves.

- Isolation etch is anisotropic; the etch will stop on the 1-1-1 plane and hence the groove depth is defined by its width. (Figure 3.5.3)

- Isolation oxidation is performed next; oxide thickness is 1.8 μ nominal for defect density reduction. See Figure 3.5.4

- Polycrystalline silicon is then deposited to a thickness of approx. 25 mils. This poly forms the substrate of the dual slice. (Figure 3.5.4)

- The original single-crystal slice is then ground away and the resulting structure is polished. The result is a largely polycrystalline slice with isolated regions of single-crystal Si. Note that both P and N type regions are available and that the N region also was an N+ buried layer. The slice has completed material fabrication at this point. Figure 3.5.5 illustrates the finished structure.

2. FRONTSIDE PROCESSING. Sequence is given below.

High Temperature Crystal Anneal
N-Base Photoresist and Oxide Etch
N-Base Diffusion
P-Base Photoresist and Oxide Etch
P-Base Diffusion
P-Emitter Photoresist and Oxide Etch
P-Emitter Diffusion - PNP Transistor Beta Piloted
N-Emitter Photoresist and Oxide Etch
N-Emitter Diffusion - NPN Transistor Beta Piloted
Capacitor Photoresist and Oxide Etch
Capacitor Low Temperature Oxidation
Implanted Resistor Photoresist and Oxide Etch
Resistor Low Temperature Oxidation
Resistor Implantation
Contact Photoresist and Oxide Etch
Sample Probe
Aluminum Evaporation
Aluminum Photoresist and Metal Etch
SIO_2 Deposition
Contact Base
SIO_2 Photoresist and Oxide Etch
Stabilization Base
Sample Probe
Backlap

- A high temperature crystal anneal follows the 1100° initial oxidation; it stabilizes the structure and reduces defects.

- N base PR and diffusion establishes the PNP base. (Fig. 3.5.6)

- P base PR and diffusion establishes the NPN base. (Fig. 3.5.7)

- P+ PR and diffusion completes the PNP device; a piloting procedure controls device beta. Contact regions for the NPN base and PNP collector are also formed at this step. (Fig. 3.5.8)

- N + PR and diffusion completes the NPN device; again, piloting controls NPN beta. PNP base and NPN collector contact regions are also formed. (Fig. 3.5.9)

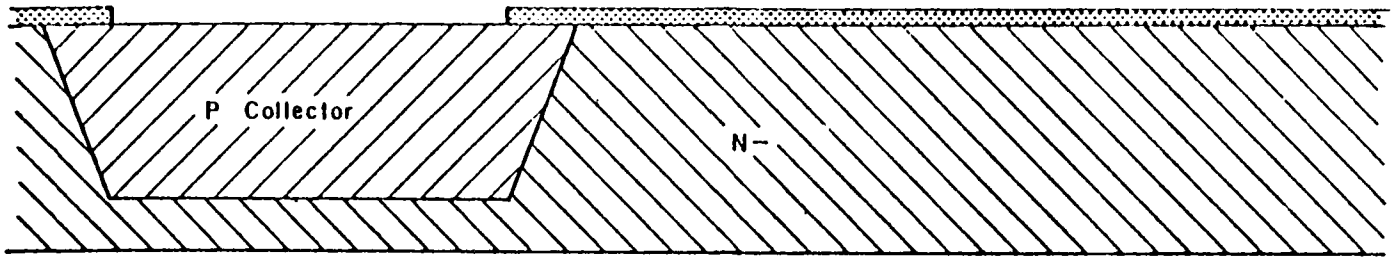
- Capacitor photoresist opens the capacitor dielectric area located over a P + diffusion used for the lower capacitor plate. A low temperature oxidation is then used to grow a precisely controlled oxide layer of 2000 Å nominal thickness. (Fig. 3.5.10)

- The implanted resistors are defined next; a thin oxide layer is grown in the resistor geometries.

- The resistor is implanted using an 80 keV boron implantation. Note the resistor end caps are P +; also the boron implantation is through a thin oxide to prevent excessive surface damage. Figure 3.5.10 gives the resistor structure. Nominal sheet resistivity is 1000 ohms/square.

-2- FRONTSIDE PROCESSING - continued

- Contact photoresist establishes apertures for ohmic contacts to the devices. (Fig. 3.5.11)
- A sample probe is performed next; device betas and breakdowns are checked.
- An E-beam evaporation of pure aluminum follows; metal thickness is 1.2 u. The layer is then delineated to form the interconnect pattern. (Fig. 3.5.12)
- A silox deposition follows; this CVD SiO_2 layer provides passivation and scratch protection. Openings to enable bonding are defined by a photoresist operation.
- A stabilization bake is next; it is followed by a detailed sample probe of device parameters and by backlap of the completed slice to a thickness of 10-12 units.



P Collector

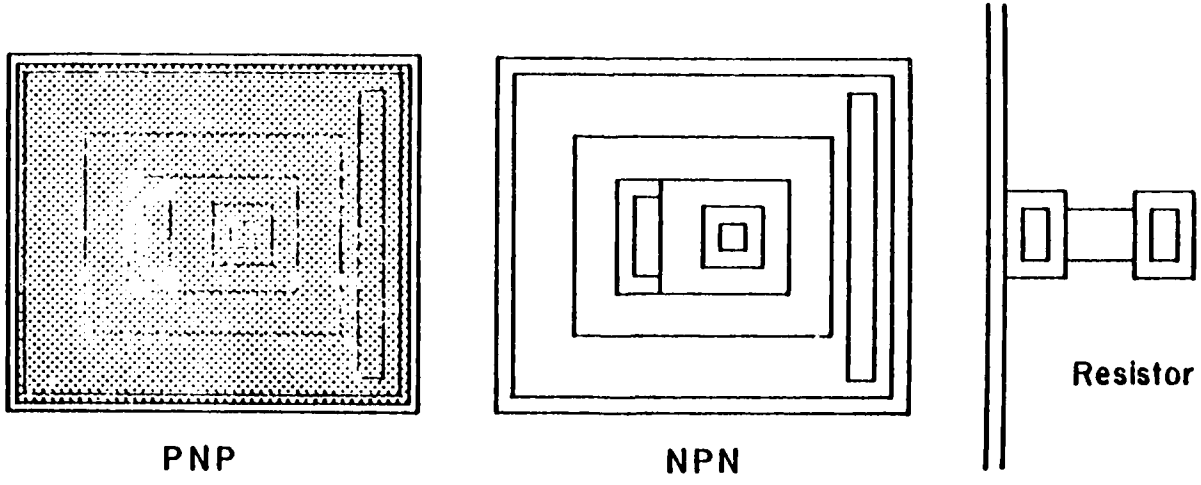


FIGURE 3.5.1

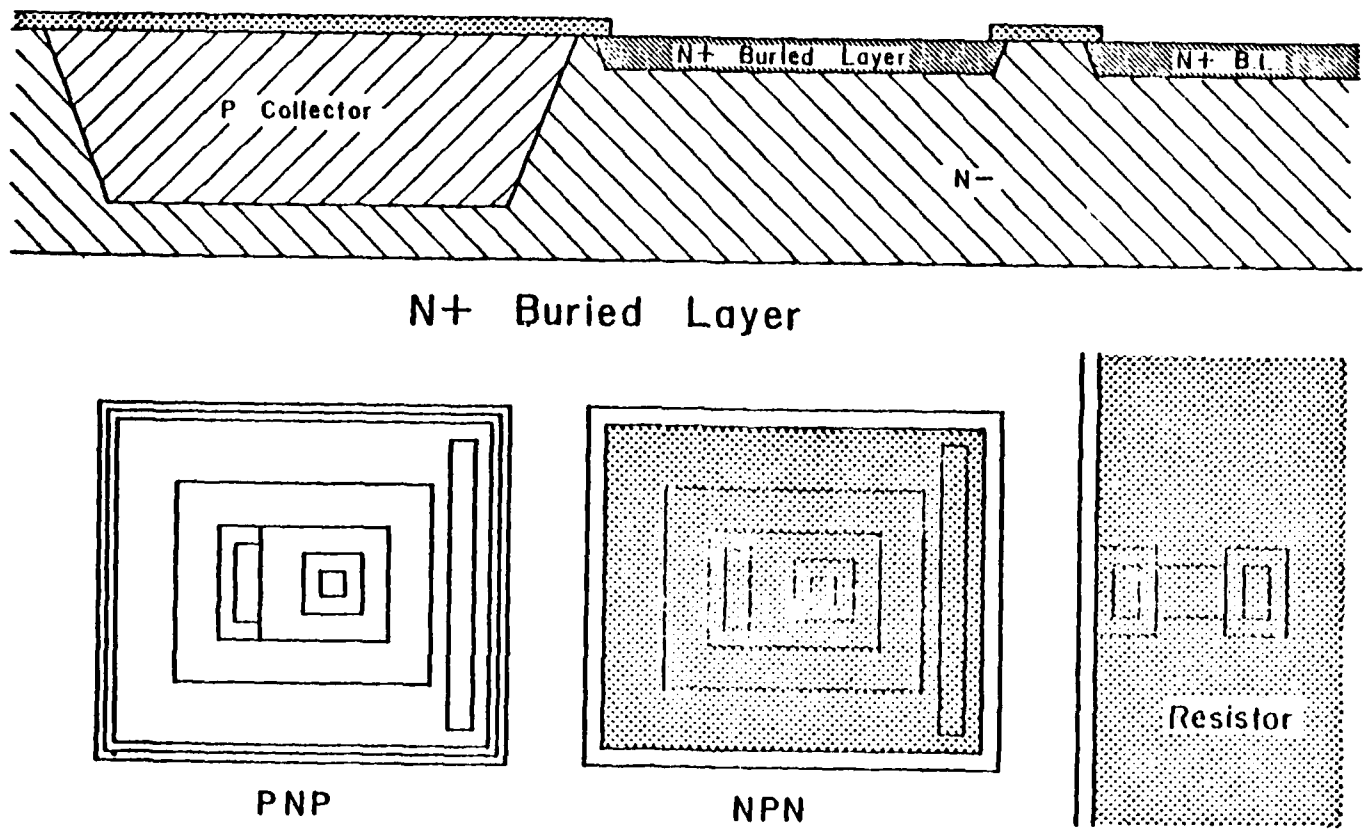

P Collector
N+ Buried Layer
N+ B.L.
N−
N+ Buried Layer
PNP
NPN
Resistor

FIGURE 3.5.2

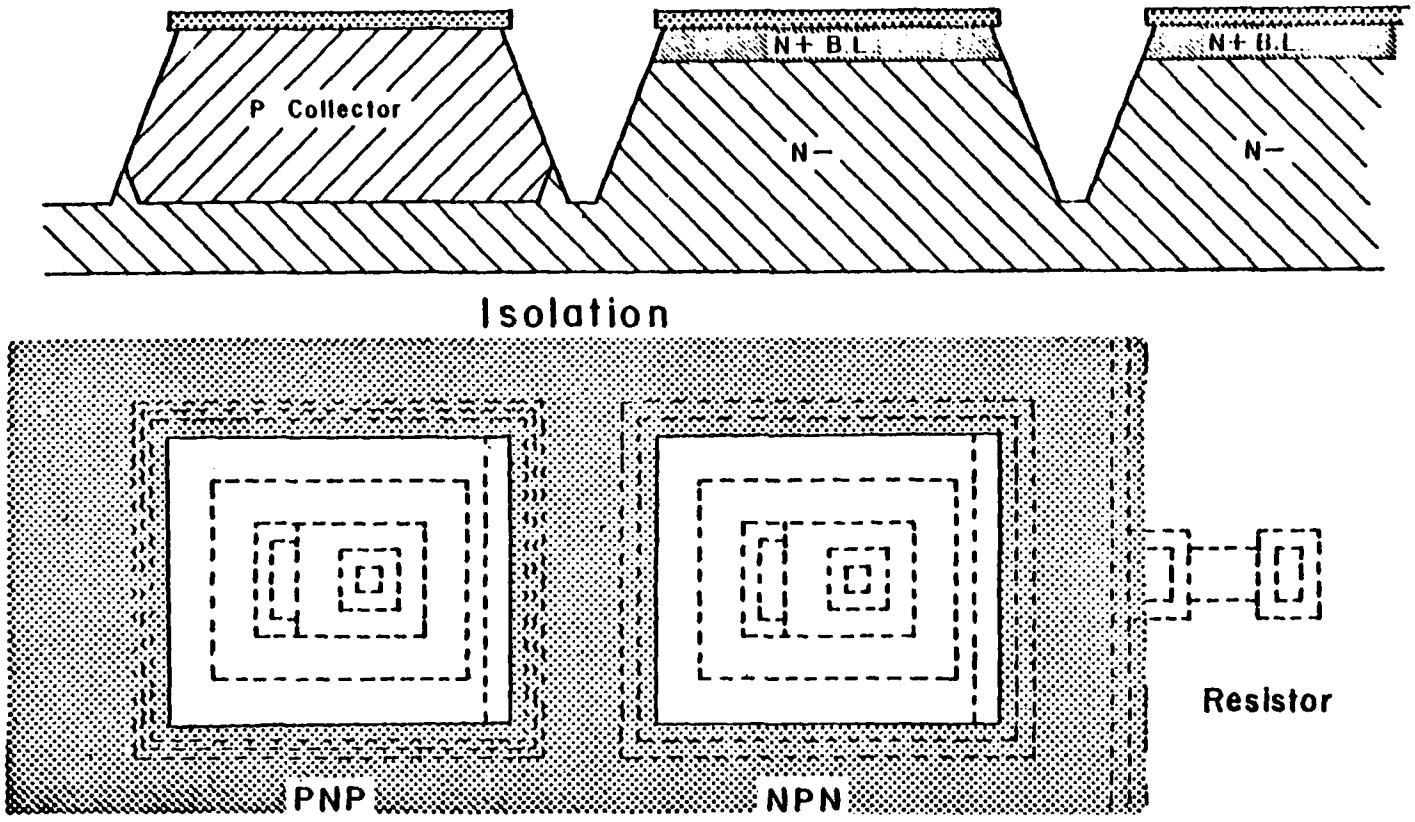
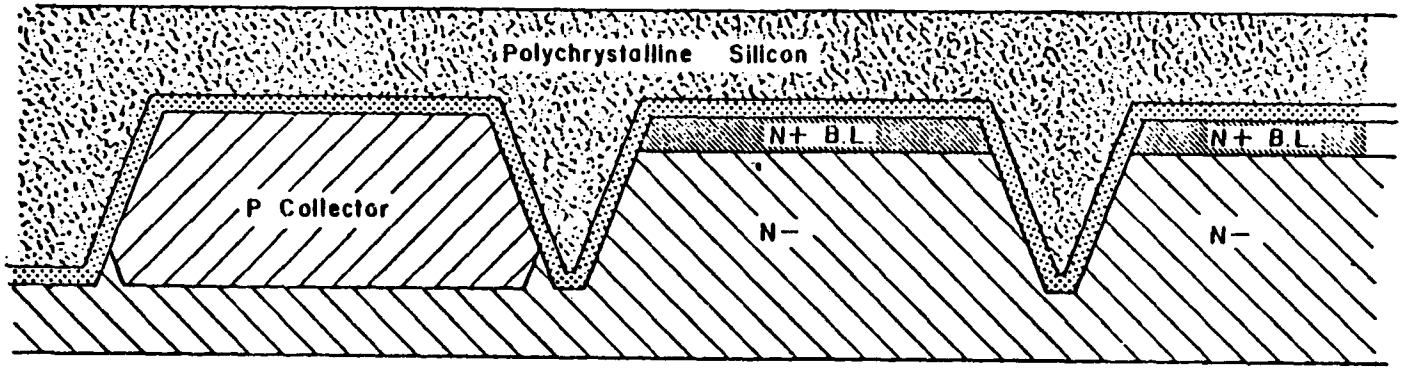
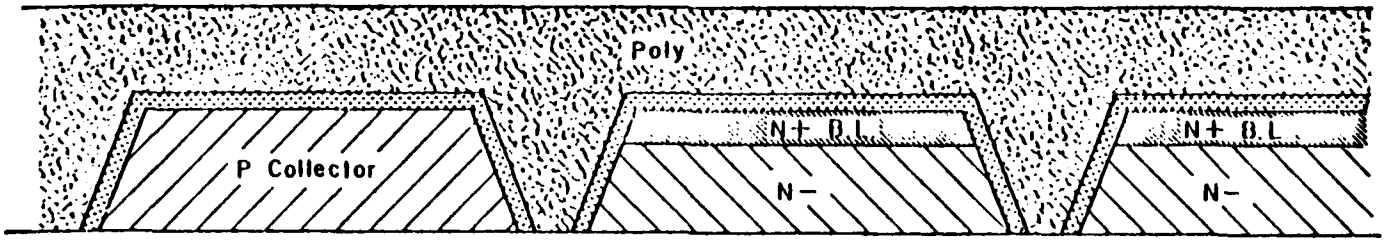


Figure 3.5.3



Grow Oxide in Moats, then add Poly for support.

FIGURE 3.5.4



Grind off excess material from N− side of slice.

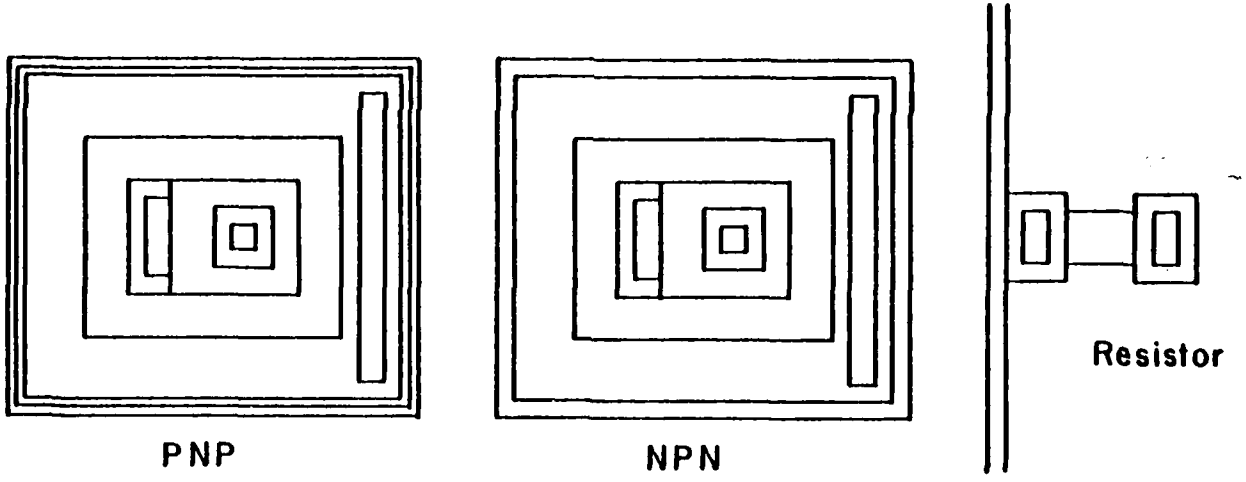


FIGURE 3.5.5

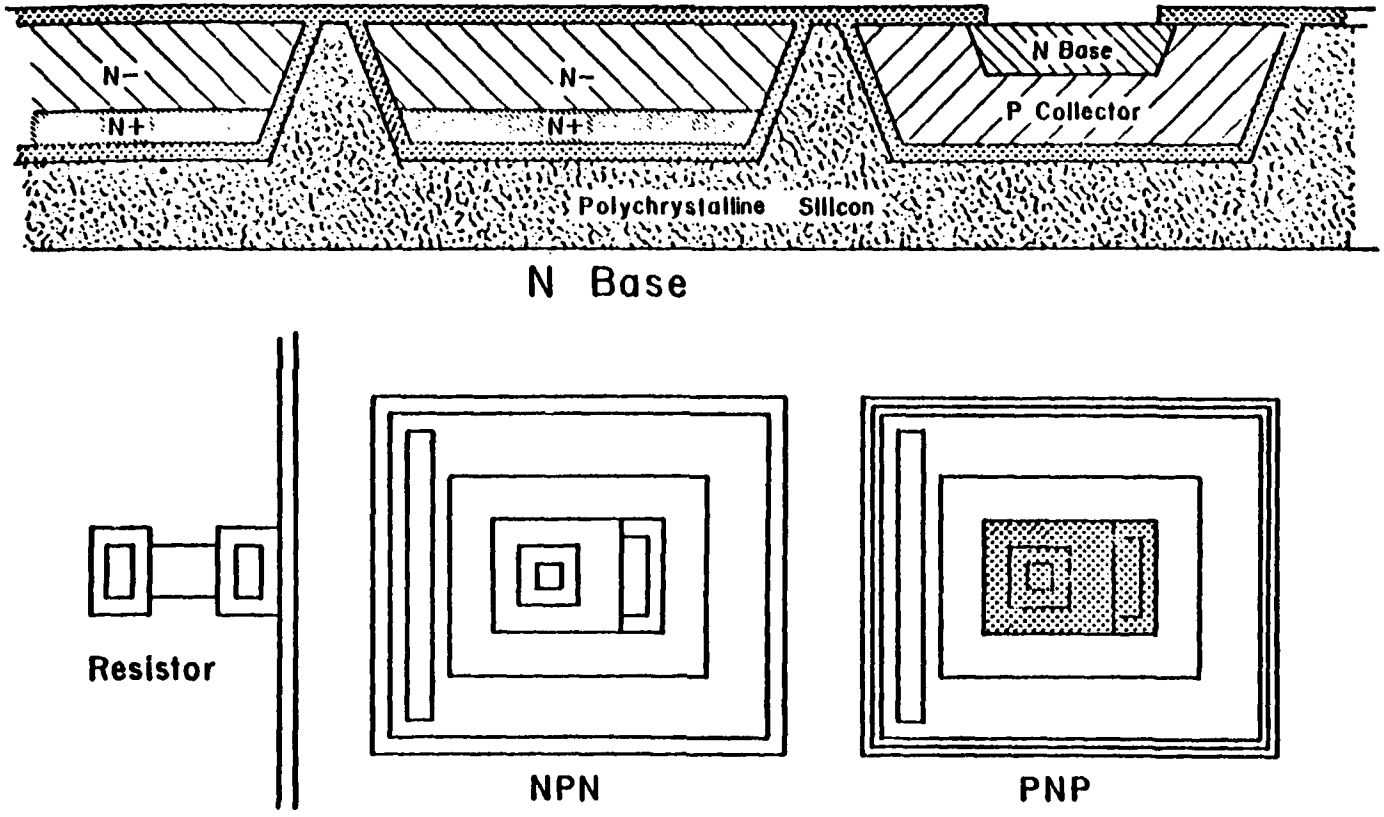

N-
N+
N-
N+
N Base
P Collector
Polychrystalline Silicon
N Base
Resistor
NPN
PNP

FIGURE 3.5.6

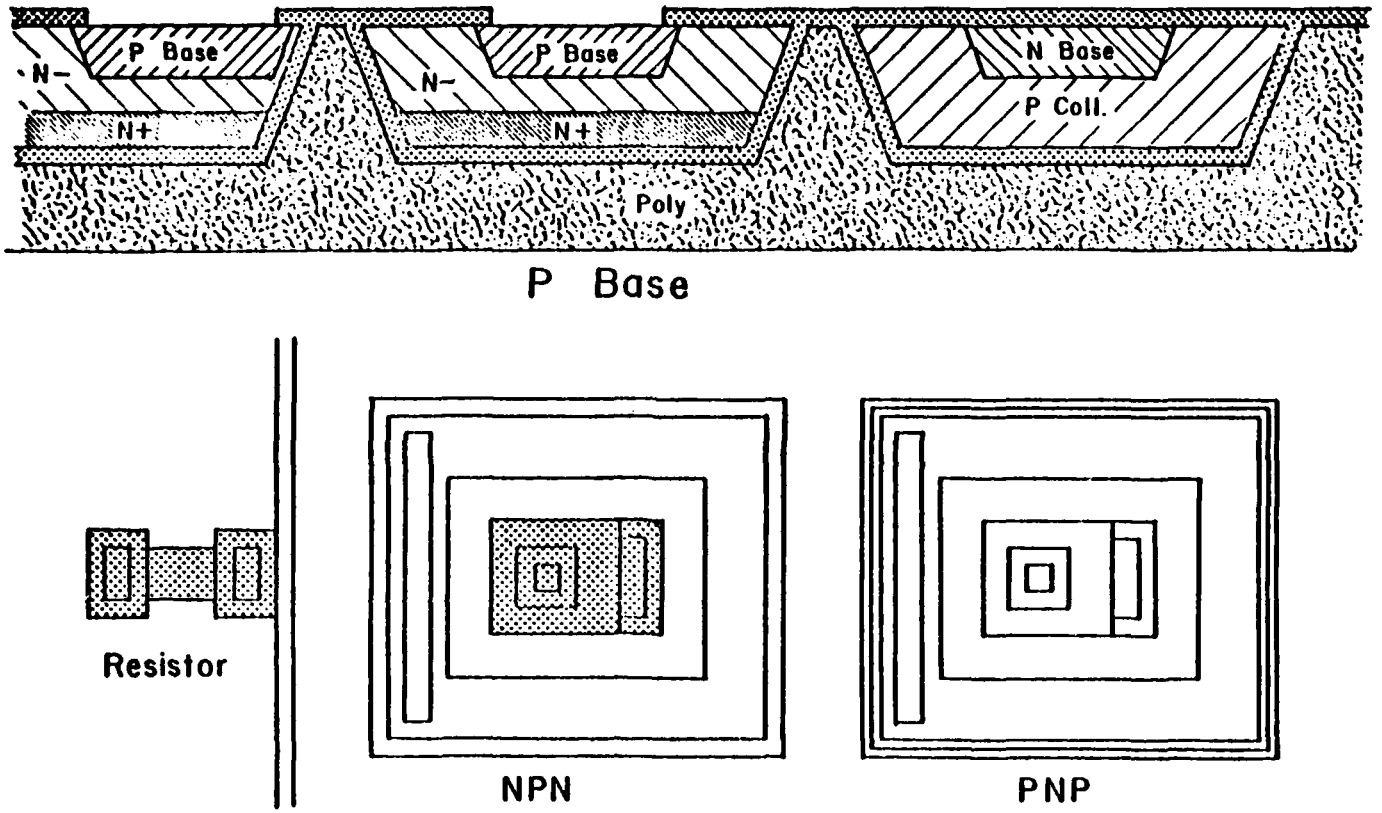


FIGURE 3.5.7

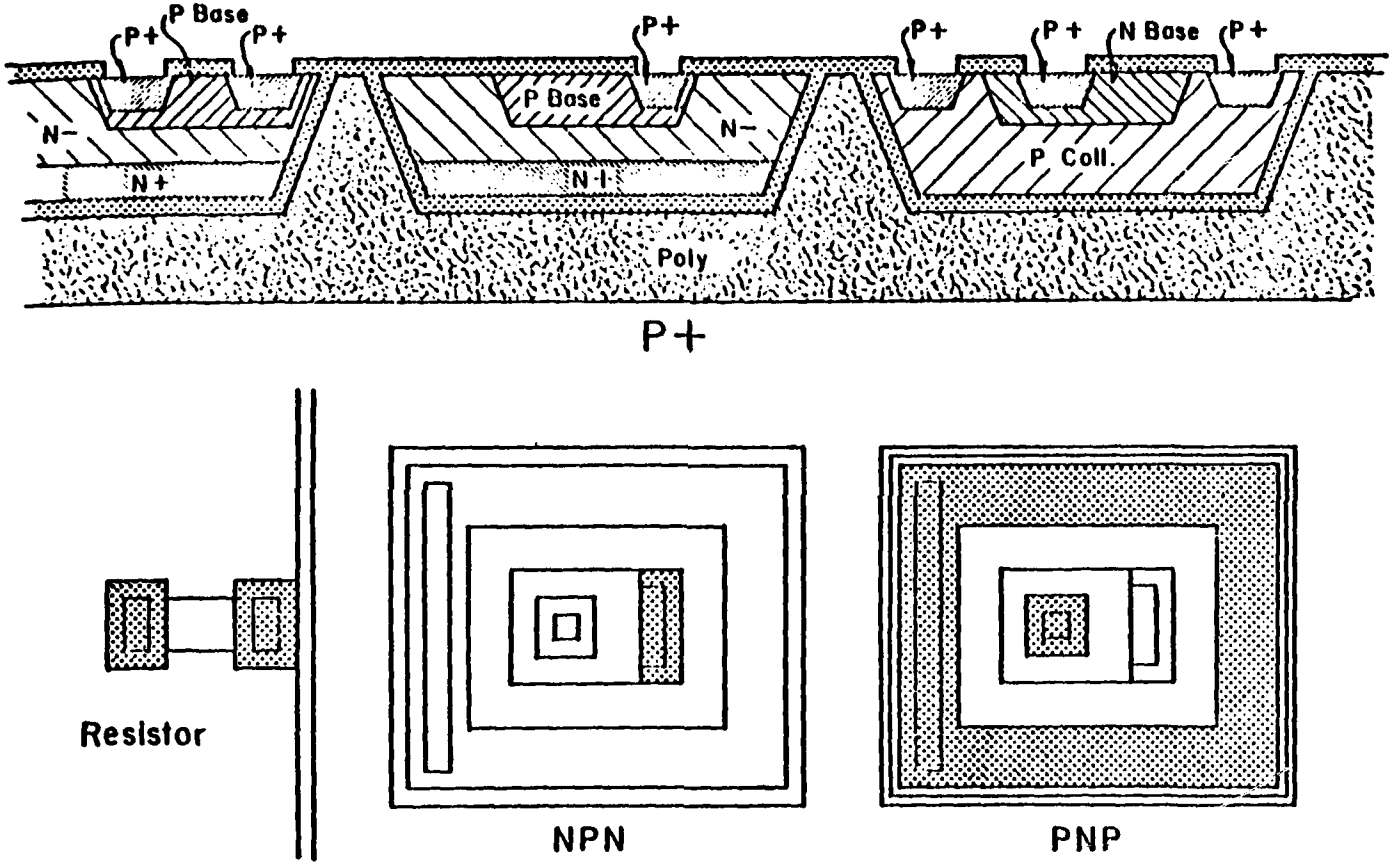

P+
P Base
P+
P+
P+
P+
P +
N Base
P +
P Base
N-
N-
N +
N +
P Coll.
Poly
P+
Resistor
NPN
PNP

FIGURE 3.5.8

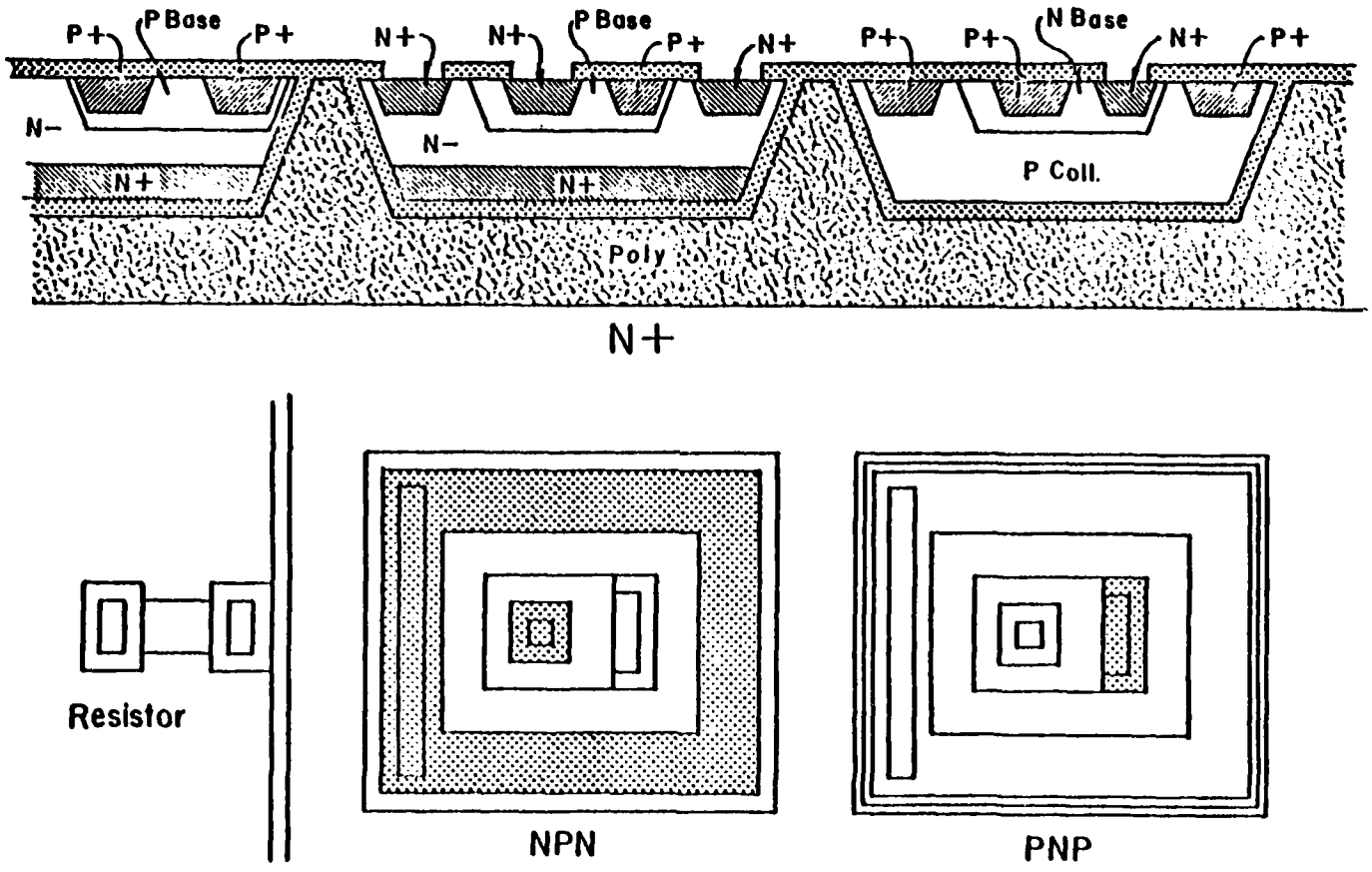
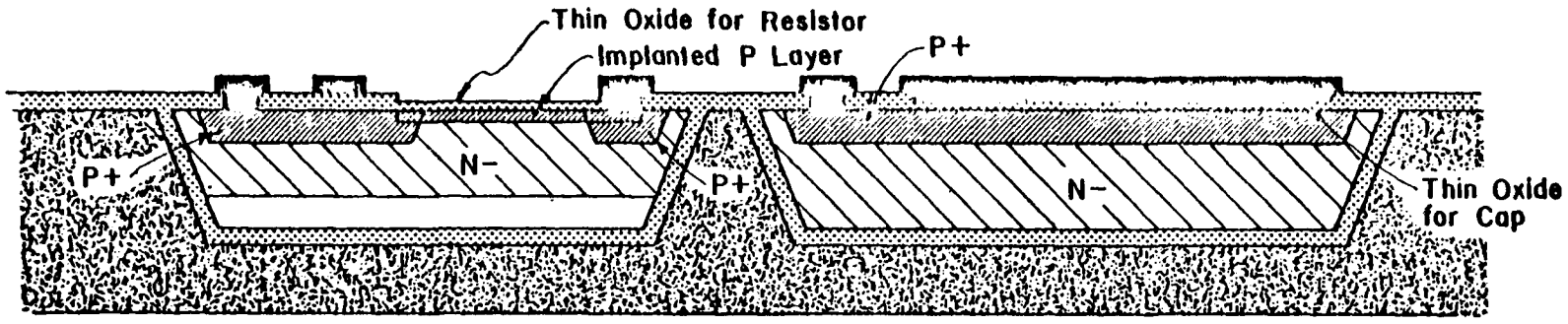
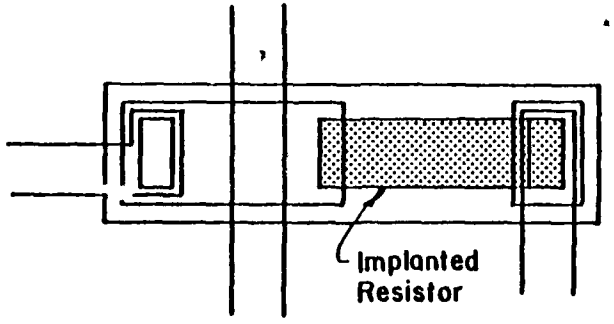
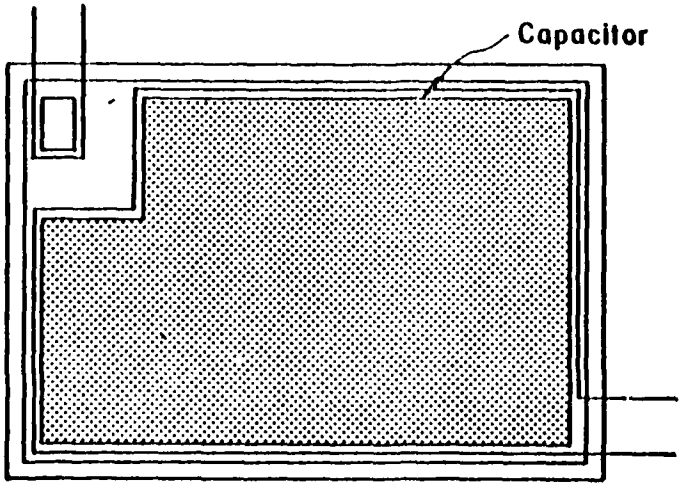

P+
P Base
P+
N+
N+
P Base
P+
N+
P+
P+
N Base
N+
P+
N-
N-
P Coll.
N+
N+
Poly
N+
Resistor
NPN
PNP

FIGURE 3.5.9



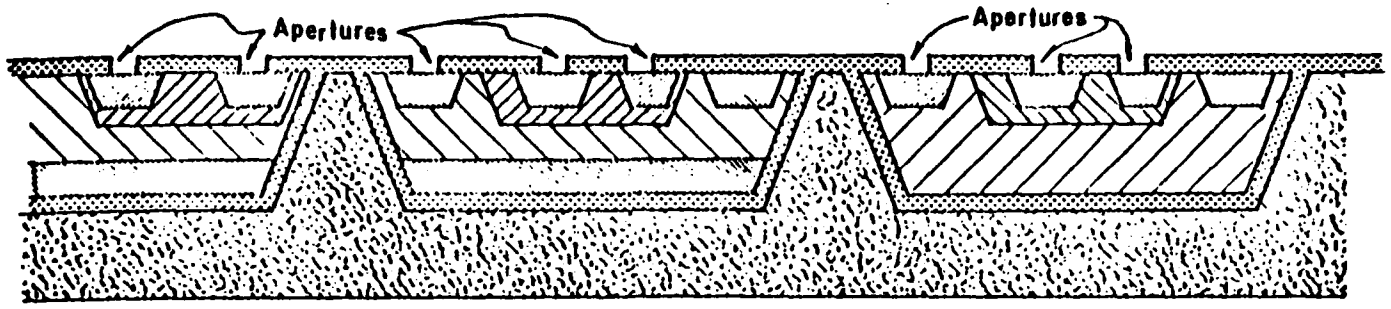


Ion Implanted Resistor



M O S Capacitor

FIGURE 3.5.10



Apertures

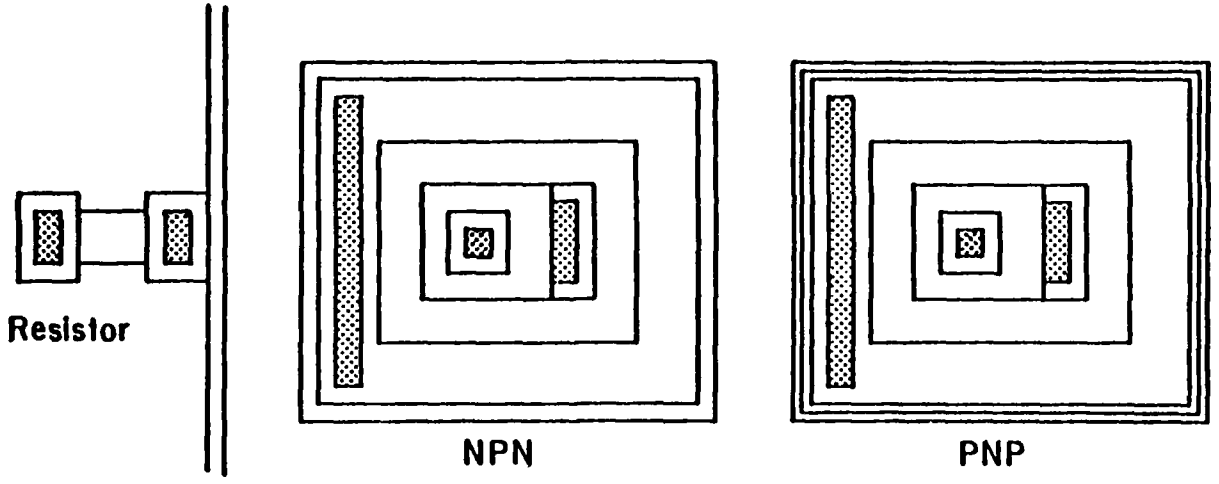
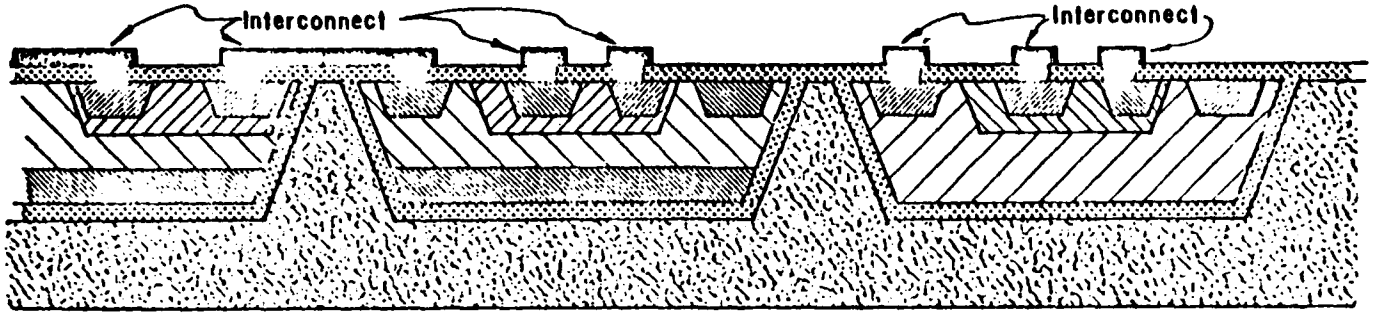


FIGURE 3.5.11



Aluminum Interconnect

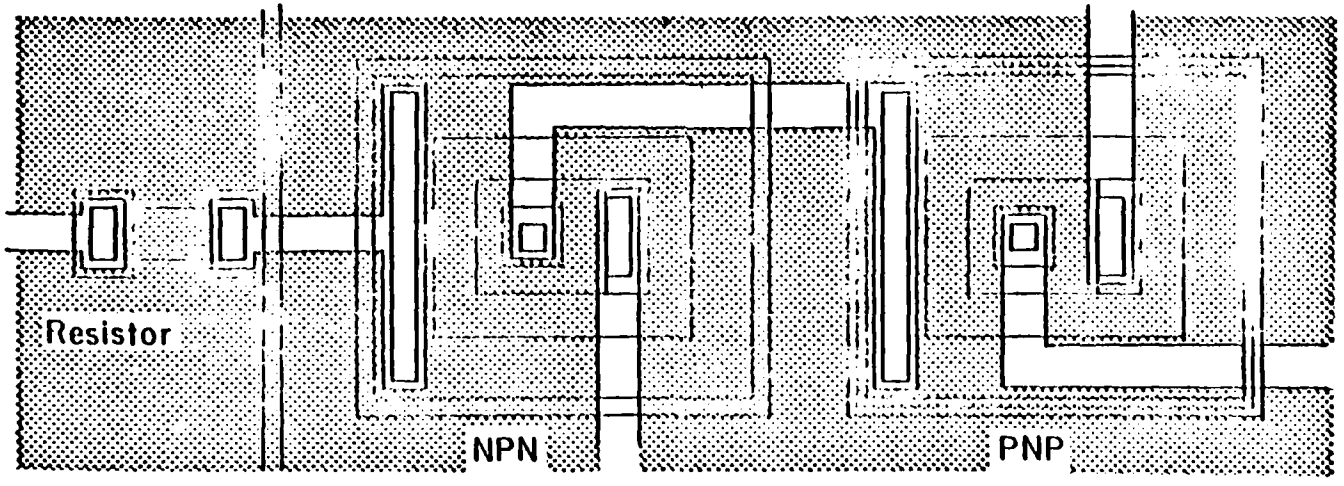


FIGURE 3.5.12

3.6 Radiation Effect Modeling

The crux of the radiation hardening effort of the DINS photopreamp lies in the structure of the two op amp stages. This structure resembles that of an advanced radiation hardened op amp now being developed by Harris' Programs Division. The fabrication of the preamp will be implemented by utilizing Harris' radiation hardened linear process.

Neutron and Total Dose Modeling

The primary effect of neutron and total dose radiation is a reduction in current gain and an increase in the resistivities of the lightly doped collector. At the radiation spec level of $, minimum betas of 30 and 15 can be expected for the NPN and PNP devices respectively. The collector resistance of NPN devices increases by a factor of four and by a factor of 1. 5 for the PNP. All post neutron computer simulations have taken these facts into account. Gummel-Poon model parameters, both pre and post radiation were used for SPICE II circuit simulation of the preamplifier under these conditions.

Transient Gamma Modeling

The predominant effect of a circuit's exposure to gamma radiation is the generation of electron-hole pairs within the space-charge regions of reversed biased junctions in the circuit. This generation of carriers causes a current, I_{pp} (primary photocurrent), to flow. These photocurrents may disrupt the normal operating conditions of the circuit sufficiently to cause a spurious output signal to be produced.

By the judicious placement of compensating reverse biased junctions on critical nodes, these photocurrent effects may be minimized. Figure 3.6.1 shows how this compensation scheme is used. Also shown are the polarities of the generated currents. In computer simulations of these photocurrents, current generators of appropriate magnitude (function of island volume) are placed in parallel with all reversed biased junctions including ion-implanted resistor islands. These islands are tied off to the more positive end of the resistor and depending on the voltage drop across the resistor, up to one half of the island volume may be depleted due to the voltage gradient set up across the resistor. With the generators in place, a transient simulation will show what effects the specified level of radiation will produce.

Computer sensitivity analyses show that the photocurrents generated by the reversed biased photodiode junctions at the input are the most critical. These are applied common mode to the preamplifier however any mismatch in photodiode volume implies a mismatch in photocurrent and this mismatch appears differentially across the input. Table 3.6.1 shows percent mismatch of photodiode volume versus signal to noise ratio. Note that this is assuming a perfect match between paired photocurrents elsewhere in the system. Also shown on Table 3.6.1 are typical signal to noise ratios for nominal system conditions.

Prompt Gamma Survival

Under very large γ environments, the major concern is to prevent either aluminum interconnect fusing or secondary junction burn-out due to surge currents (assuming all devices become shorts). This is accomplished in the preamplifier design by using limiting resistors RLIM1 through RLIM9. These are N+ resistors with a pre-radiation value of 50 ohms.

The secondary concern is the part's recovery time after such an event. A worst-case computer simulation has been performed using photo-current sources generating 100 milliampere, 100 nanosecond wide pulses across every reversed biased junction in the circuit. The result of this simulation is shown in Figure 3.6.2. Under this condition, recovery time is in the order of 10 microseconds.

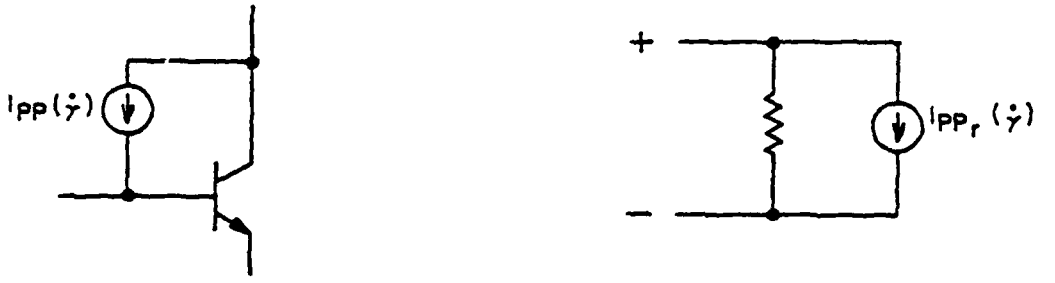
$\dot{\gamma}$ COMPUTER MODELING

THE GAMMA RADIATION CURRENT CAN BE CALCULATED FROM THE FOLLOWING EXPRESSION:

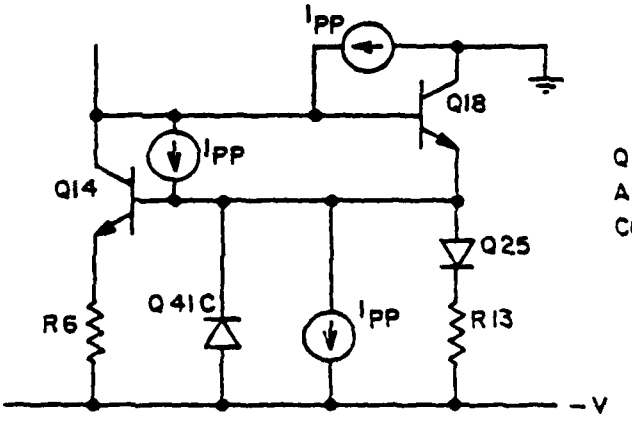
$$I_{PP}(\dot{\gamma}) = qg_o \text{ Vol. } \dot{\gamma}$$

WHERE $g_o = 4 \times 10^{13}/\text{rad-cm}^3$

COMPUTER MODELS



TYPICAL COMPENSATION SCHEME



Q14 COMPENSATES Q18
AND Q41C IN TURN
COMPENSATES Q14

Figure 3.6.1

TABLE 3.6.1

Assumptions:
- Minimum input laser signal of 300 NW and spec radiation.
- Four megohm nominal transimpedance
- .44 amp/watt photodiode responsivity
- 8.25 ua photodiode photocurrent
- All other matching is absolute

Signal to Noise Ratio	% Mismatch in Photodiode Volume
1.6 to 1	1%
.8 to 1	2%
.53 to 1	3%
.4 to 1	4%
.32 to 1	5%

Under typical system conditions of twice the worst case minimum laser signal and a gamma rate level one order of magnitude less than the specification level.

Signal to Noise Ratio	% Mismatch in Photodiode Volume
32 to 1	1%
16 to 1	2%
10.6 to 1	3%
8 to 1	4%
6.4 to 1	5%

PROMPT GAMMA RECOVERY TIME

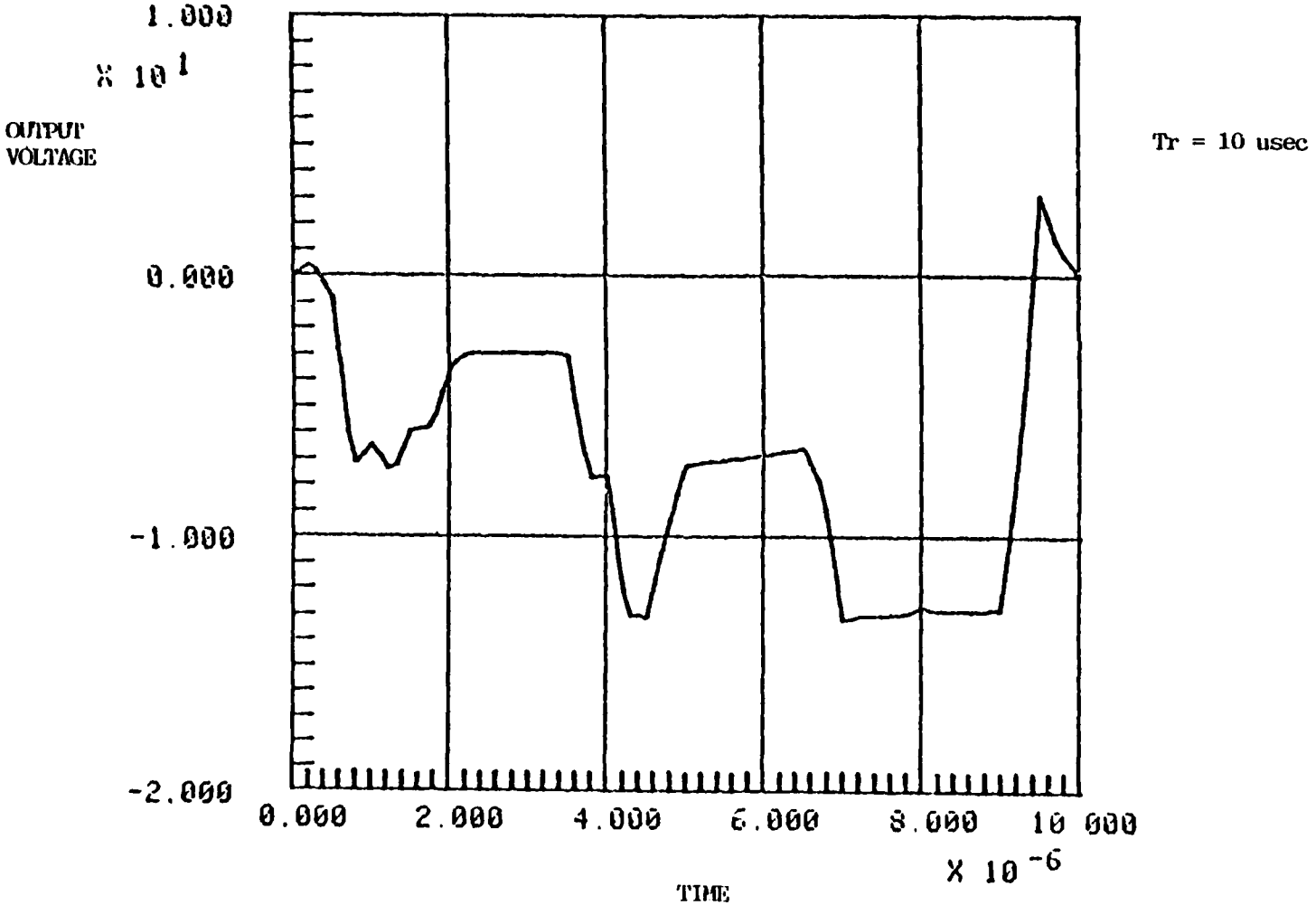


FIGURE 3.6.2

3.7 Thermal Noise Analysis

As previously stated, the noise signal generated as a result of a transient gamma event is the largest noise contributor in the system. However, for completeness a thermal noise analysis was performed over temperature to insure that these components were negligible. The simulation results showed the total output thermal noise voltage to be two orders of magnitude less than that generated by a 1% mismatch in photodiode volume. At 25°C the output noise voltage was 7 millivolts, 8.77 millivolts at 125°C and 6.5 millivolts at -55°C.

4.0 CIRCUIT DESCRIPTION

4.1 General Overview

Shown in Figure 4.1 is the schematic diagram of the preamplifier. As mentioned earlier, the overall structure is that of two similar radiation hardened op amp stages in cascade. There are some variations between the two due to different gain-bandwidth products, stability requirements and short circuit protection requirements.

The transimpedance gain of the first stage A_1 is 30K and is set by feedback resistor RF1. Its closed loop bandwidth is set by the closed-loop pole obtained between RF1 and lead compensation capacitor CF. The bandwidth is a nominal value of 2 megahertz. Elements R15 and CIN are used to match the impedance seen at both input ports. This is important in order to minimize current induced voltage offset and also to balance the photocurrents generated at the input by these resistors. The open loop bandwidth of A_1 is set by CCOMP1 and the gm of the input stage, using the classical dominant pole approach. It is a nominal value of 8 megahertz. Only 2 megahertz was required for the gain-bandwidth product of A_1 (voltage gain is unity in this stage) however any further reduction would require a larger value CCOMP1. At its present value, the phase margin of the stage is greater than 45°. The value of CCOMP1 is 50 pf (relatively large). Any further lowering of gm will increase the amplifier's photocurrent sensitivity due to the reduction in operating current in the input differential pair.

Figure 4.1 also shows the input photodiode D_L, and the compensating masked photodiode D_D. D_D is required to provide matched (common-mode) photocurrents to the preamplifier during a transient gamma event. D_D also assures a match in impedances seen by both input terminals. During circuit simulations both photodiodes were modelled as capacitors whose value was the sum of the diode's depletion and isolation capacitances. A worst case figure of 6 pf was used.

The second stage A_2 is a non-inverting amplifier in a gain of 133. The closed loop voltage gain is set by

$$\frac{RF2 + R31}{R31}$$

Resistor R32 matches the impedances seen by both input ports of A_2. This resistor shall be a P+ resistor thereby generating very low radiation currents.

There are four ion-implanted resistors in the circuit whose islands shall not be tied off to the more positive side of the resistor. These are R15, RF1, RF2 and R31. Depending on the offset condition of A_1 and A_2, these resistors may have voltages of either polarity across them. If they were tied off one could establish a forward biased junction between the P implant and the N - island.

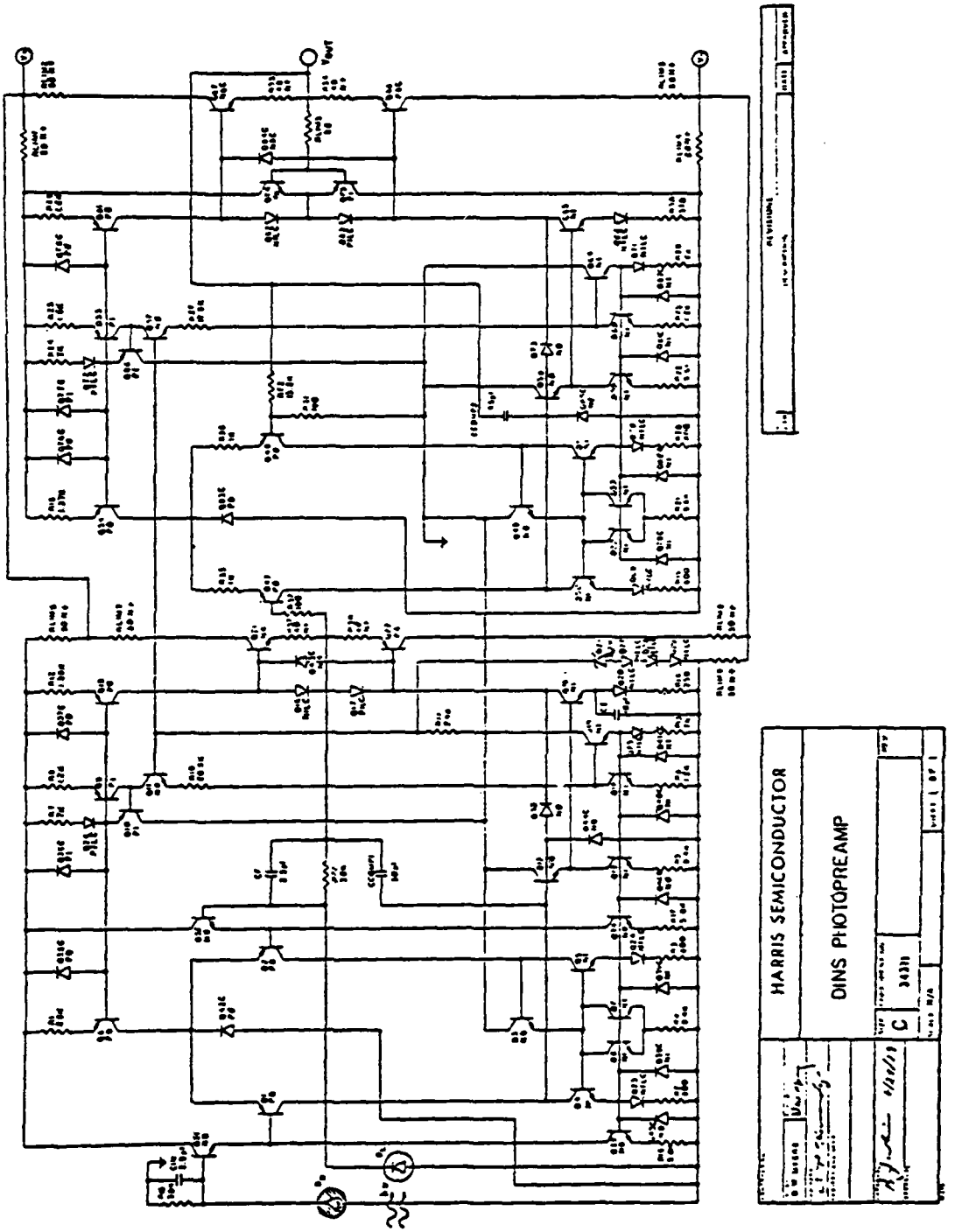


FIGURE 4.1

The case of resistors RF2 and R31 is more complex. These two resistors have significantly different values (RF2 = 13.2K and R31 = 100 ohms) however since they set the gain of A_2 they must ratio. In addition, their photocurrent generation must be mutually compensating in order that no differential voltage appears at A_2's input. The approach that was chosen dictated RF2 to be built as eleven 1.2K series connected resistors in separate islands and R31 to be twelve 1.2K parallel connected resistors in separate islands. This resolves the ratio tracking problem but leaves R31 generating twelve times the photocurrent of RF2. This was resolved by paralleling eleven dummy islands, whose volume matches that of a 1.2K resistor, with RF2. A summary of this compensation scheme is shown in Figure 4.2.

A gain of 133 for A_2 implys this stage must have a gain-bandwidth product of greater than 250 megahertz. This figure would be unreasonable if the amplifier were required to be stable at a closed loop gain of unity. However at a gain of 133, greater than 45 degrees of phase margin has been achieved. Emitter degeneration resistors R35 and R36 tend to reduce the gm of the input stage. However they are required to aid in the stability of A_1. The gm of A_2's input stage is

$$gm = \frac{1}{R35 + 2\,\frac{KT}{q \cdot I \cdot Q47}}$$

The collector current of Q47 is 185 microamps and therefore gm is 780 microhms Gain-bandwidth product is defined as

$$GBW = \frac{gm}{2\pi C}$$

Here C is element CCOMP2 or .45 pf therefore the gain-bandwidth product of A_2 is 276 megahertz.

When reading the system schematic, all device names with a trailing C in the name are photocurrent compensation devices and are reverse biased.

TABLE 4.1 lists gain-bandwidth requirements, actual total power dissipation and actual pre and post radiation steady-state output voltages.

4.2 Biasing

Both stages A1 and A_2 are biased from a common voltage reference consisting of D21, Q27, Q28 and Q29 however each stage maintains its own isolated NPN and PNP base biasing rails. R24 sets up a current of 275 ua to bias the zener ON. Devices Q11 and Q57 then set up reference currents for the four independent base rails located at the bases of Q9, Q14, Q55 and Q60.

4.3 Input Stages

The inputs stages of A1 and A_2 differ in structure. For A_1 an NPN/PNP modified Darlington configuration was chosen (Q31-Q1 and Q32-Q2). The necessity for this type of configuration here is due to post-neutron bandwidth reduction due to a lowering of gm. The expression for gm of a differential pair is

$$gm = 2\left[\frac{1}{\frac{r_o + Rs + r_e}{\beta_n}}\right]$$

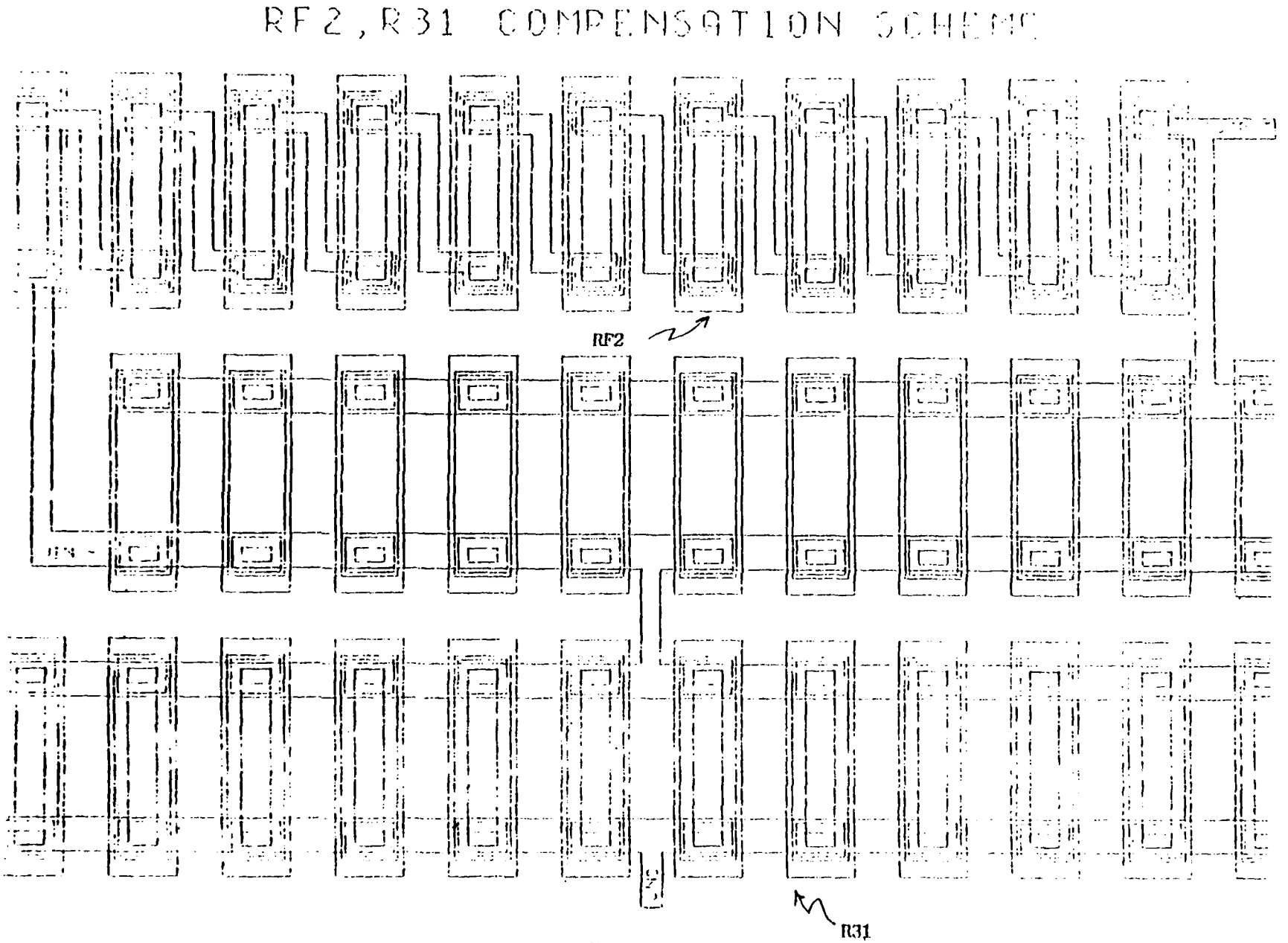


FIGURE 4.2

TABLE 2

TABLE OF ELEMENT VALUES

----- RESISTORS -----

NAME	VALUE
R1	2.50E+03
R2	8.00E+02
R3	8.00E+02
R4	8.40E+03
R5	8.40E+03
R6	1.20E+03
R7	7.00E+03
R8	1.20E+03
R9 (RF1)	3.00E+04
R10	2.05E+04
R11	2.40E+04
R12	1.35E+03
R13	7.00E+03
R14	2.50E+02
R15	3.00E+04
R16	5.90E+03
R17	5.80E+03
R18	1.27E+03
R19	8.00E+02
R20	8.00E+02
R21	9.60E+03
R22	9.60E+03
R23	1.20E+03
R24	7.00E+03
R25	1.50E+03
R26 (RF2)	1.32E+04
R27	1.75E+04
R28	1.60E+03
R29	7.00E+03
R30	3.70E+02
R31	1.00E+02
R32	1.00E+02
R33	4.00E+01
R34	4.00E+01
R35	1.00E+03
R36	1.00E+03
R37	4.00E+01
R38	4.00E+01
RLIM1	5.00E+01
RLIM2	5.00E+01
RLIM3	5.00E+01
RLIM4	5.00E+01
RLIM5	5.00E+01
RLIM6	5.00E+01
RLIM7	5.00E+01
RLIM8	5.00E+01
RLIM9	5.00E+01

----- CAPACITORS -----

NAME	VALUE
CCOMP1	5.00E-11
CF	2.50E-12
CE	1.00E-11
CCOMP2	4.50E-13
CIN	2.50E-12

TABLE 4.1

ELECTRICAL PERFORMANCE

GBW	REQUIRED	ACTUAL
A_1	2 mHz	8 mHz
A_2	266 mHz	276 mHz

ACTUAL POWER DISSIPATION (Two Channels)	TEMPERATURE
212 Milliwatts	25°C
220 "	125°C
208 "	-55°C

AC STEADY-STATE OUTPUT VOLTAGE
(Assuming no offsets)

PRE-RAD V out (SS AC) = 526 Millivolts

POST-RAD (Neutron Spec) V out (SS AC) = 519 Millivolts

These outputs were obtained based on a minimum 300 nanowatt laser signal and a photodiode responsivity of .44 amps/watt. The corresponding steady state AC input signal used was 132 nanoamperes.

Where rb is the base spreading resistance, re is the dynamic input impedance and R_S is a source impedance. For a radiation insensitive gm it is desirable that the second term be dominant since it is not beta dependent. If a simple differential pair were used, R_S would actually be R15 or RF1 (30K). Therefore under post radiation conditions, betas would not be large enough to adequately swamp out this term. Using the Darlington approach, the gm expression is

$$gm = \frac{1}{2\left[\frac{r_{b1} + R_s + r_{b31}}{\beta_D \beta_n} + r_{e1}\right]}$$

and the R_S term now is effectively buffered.

The input stage of A_2 sees a low source impedance. At the non-inverting input this consists of R32 in series with the output of A_1 and approximately R31 in parallel with RF2 at the inverting input. Therefore a simple differential pair was chosen. Upon initial simulation of the open loop gain of A_1 a 10 DB gain peak was detected around 50 megahertz. The peak was caused by the fact that at 50 megahertz the feedback factor of A_2 was low enough that A_2's input impedance began to look capacitive. At the same time, at high frequencies, the impedance looking into the emitter of a follower stage emulates an inductor. This creates a now well known tank circuit effect. Two changes were the key to the removal of the peak to obtain the smooth roll-off characteristics presently seen. First, emitter degeneration resistors R35 and R36 were used to increase the [illegible]urt of A_2's input impedance. Second, capacitor CE in A_1 in parallel with the dynamic impedance of Q20 plus R14 generates a zero in the transfer function. The combined effect of these two elements assures the stability of A_1 with a simulated phase margin of 65 degrees.

4.4 Active Loads and Gain Stages

The input stage current mirrors used in A_1 and A_2 are modifications of the classic Widlar current mirror. In A_1 devices Q3-Q4-Q5-Q6 and Q7 form the mirror. Q5 is essentially diode connected by the base-emitter junction of Q3. The parallel combination of Q6-Q7 draw out Q3's emitter current from the base rail of the mirror. Note that devices Q6 and Q7 have the same areas as Q4 and Q5 and therefore serve as photocompensation devices. Device Q12 serves as a buffer between the mirror and the gain stage Q19. Q12 is biased at the same current as Q3 so the base currents they rob from the collectors of Q4-Q5 are equal.

Q12 and Q19 form the gain stage of A_1. Capacitor CCOMP1 performs the pole-splitting action of the integrator. Note that this capacitor ties to the output of A_1 and not to the collector of Q19. Simulations show a greater degree of phase margin is achievable using this approach.

4.5 Output Stage and Short Circuit Protection

Both A_1 and A_2 use the standard class AB output stage found on most op amps used today. The output stage of A_2 differs from that of A_1 in operating current and device size. Also, A_2 incorporates a short circuit protection scheme using Q74 and Q75. Since system specifications required A_2 to drive a

coaxial cable, a parallel RC load was used throughout the simulations. The value of R was 2K and C was 100 pf. The large output devices and operating points help source and sink the larger currents necessary to drive such a load.

Under short circuit conditions, large currents may initially flow through resistors R33 or R34 (depending on the direction of the short). If the drop across R33 reaches one diode drop, device Q75 turns on and robs driving current from the gain stage. A similar condition of opposite polarity causes a similar effect from R34 and Q74.

4.6 Breadboard Simulation Results

Shown in Figure 4.3 is the block diagram of the breadboard version of the photopreamplifier. For the transimpedance stage, the afore mentioned radiation hardened op amp (913) was used. This part is internally compensated and has a gain bandwidth product of 10 megahertz. For this reason it was not feasible to use this op amp for the second stage since in the breadboard version this stage requires a gain bandwidth product of 100 megahertz (BW = 1 mHZ at a gain of 100). Instead, a commercial op amp, the HA5190 manufactured by Harris' Products Division was used. This part has a gain bandwidth product of 150 megahertz but is not radiation hardened.

The purpose of constructing the printed-circuit board version of the system was to see if the required overall transimpedance of 3 megohms and a 1 megahertz bandwidth could be achieved without instability. Also the circuit was to be used to amplify signals from prototype photodiodes whose fabrication was near completion. The results achieved were very good. A spectrum analyser showed the gain at 3.1 megohms and a bandwidth of 1.5 megahertz. The laser light used to drive the photodiodes was modulated by a 100 kilohertz square wave using a quartz modulator and the diodes output was properly amplified by the breadboard preamplifier.

DINS PHOTOPREAMP BREADBOARD

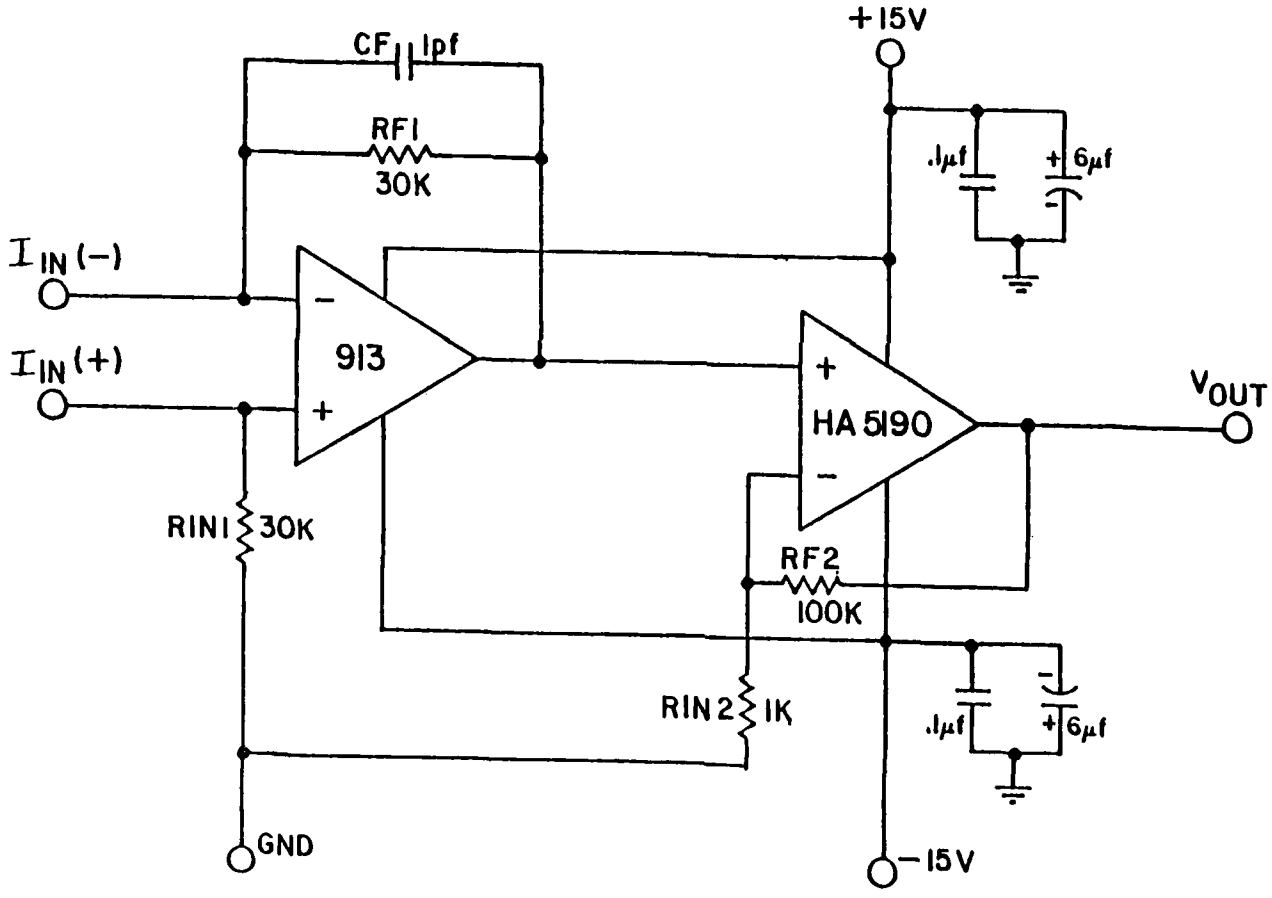


FIGURE 4.3

5.0 TOPOGRAPHICAL DESIGN

5.1 Photodiode Layout

A test chip was designed with various geometry photodiodes to determine an optimum performance design compatible with existing process capabilities. Three pairs of diodes were designed on the test chip; a pair consisting of an open diode for detecting a 6328Å He-Ne laser and an identical geometry dark diode, masked from the laser with aluminum, for radiation photocurrent compensation. This section describes the three designs and the advantages and disadvantages of each.

Photodiode Design #1: Stepped D.I.

Figure 5.1.1 shows the stepped D.I. design. The dielectric isolation pattern of this design was stepped, anticipating that the natural corner rounding which occurs during the anisotropic silicon etch (moat etch) would result in a circular shaped island. However the etch time required to etch the shallow island (0.2-0.3 mil) resulted in only minimal corner rounding. As a result, the final island geometry closely replicates the drawn island geometry as shown in the design.

The anode is a 5.0 mil radius semicircle with 0.2 mil spacing between the anode aperture and the minimum D.I. island. P+ contact to the anode is made via a 0.6 by 9.0 mil aperture along the diameter of the semicircle. The N+ contact to the cathode is a 0.6 mil aperture spaced 0.3 mil from the anode aperture.

Photodiode Design #2: Stepped D.I. with N+ Ring

The stepped D.I. with N+ ring design is shown in Figure 5.1.2. Additional steps were added in the dielectric isolation pattern to determine if the corner rounding effect with the additional steps would result in a more uniform semicircular pattern. However as in the previous design the minimal required etch time resulted in the final island geometry being very similar to the design island geometry.

The anode of the design is identical to the previous design.

A 0.4 mil N+ ring spaced 0.3 mil from the anode was designed for the cathode contact. This ring provides a lower resistance cathode contact to enhance the efficiency of the diode. The disadvantage of this design is that the addition of the N+ ring increases the total island volume over the previous design which could result in an increase in radiation induced photocurrent. The trade-off to be evaluated then is improved photodiode performance vs. radiation hardness.

Photodiode Design #3: Circular D.I. Island

The circular D.I. island design is shown in Figure 5.1.3. This design was included to study the feasibility of anisotropically etching a circular pattern at the dielectic isolation photoresist and moat

No significant problems were encountered on the first run at the D.I. photoresist and moat etch steps. In fact the final island geometry was very close to the design geometry.

The anode, anode contact and cathode contact were identical to Design #1.

Results of responsivity testing and generation volume tradeoffs showed the second of the above geometrics to be optional. To save on design time and to enable use of existing D.I. material the dual photodiode chip used a metal and silox level redesign of the test chip. Added to the chip were four 30KΩ feedback resistors using a 1000 ohms/square shallow baron implanted resistor technology. To prevent photoeffects in these resistors, they are covered with an aluminum shield.

The Harris mask number for the photodiode is 1061. The chip is laid out in English units. The chip site is 98 X 77 resulting in approximately 830 dice per 3" slice. The following levels make up the photodiode mask set:

Level	Level Name
106101	Isolation
106108	N+ buried layer
106110	N+ cathode contact
106116	P+ anode contact
106131	Apertures
1061	Implanted resistors
1061	Anode
1061	Nitride
1061	Metal
1061	Silox

NOTES:

1) The isolation level creates the V-grooves used in D.I. fabrication.

5.2 Amplifier Layout

The preamplifier chip is laid out using standard D.I. ground rules which will be discussed in detail. The chip is divided into two identical channels. Accurate gain and balance matching is realized by multisigmented feedback resistors also, separate VCC, VEE, and ground lines are provided for each channel to match impedances and prevent oscillation.

Thermal gradient matching is also important. Each section of the two channels is laid out around lines of thermal symnetry. Also the large, heat producing output transistors are placed at the far side of the chip from the photodiode connections.

The bond pads are laid out down one side of the chip to facilitate direct bonding to the photodiode chip, since the preamplifier circuit provides the VEE and ground to the photodiode and receives

the photodiode output for amplification.

For reference, Figure 5.1.4 provides a technical diagram of the photodiode/amplifier system. Figure 5.1.5 illustrates the bonding pad layout; Figure 5.1.6 is a photograph of both chips.

The Harris mask series number for the DINS Preamplifier is 105800. This was the first Harris circuit to be laid out entirely in metric dimensions. The chip size is 3810 X 2921 micron, resulting in approximately 340 dice per 3" wafer. The following levels make up the amplifier mask set:

Level	Level Name
105801	Isolation
105804	P Collector
105806	N+ buried layer
105816	N base
105821	P base
105826	P+ emitter
105831	N+ emitter
105833	Capacitors
105835	Implanted resistors
105836	Oversize resistors
105837	Apertures
105839	Oversize apertures
105850	Metallization
105856	Silox
105857	Oversize silox

NOTES:

1) The isolation level is used to cut the V-grooves necessary for tielectric isolation fabrication.

2) The oversize levels are used in double coat/double expose photo resist operations for defect density reduction.

Layout Ground Rules

The preamplifier layout has both NPN- and PNP- transistors, base and ion-implanted resistors, and a zener diode. One channel of the circuit was laid out entirely and then mirror-imaged to form the second channel. Detailed ground rules used in this layout follow:

1.0 GENERAL RULES

1.1 All dimensions in microns unless otherwise specified.

1.2 All dimensions minimum unless otherwise specified.

1.3 All devices (both active and passive) in separate D.I. islands.

1.4 All bond pads in separate D.I. islands.

2.0 SPECIFICATIONS

2.1 Starting material is 3-5 ohm-cm, 1-0-0 orientation.

2.2 Finished island thickness range is 17.8 - 28μ.

2.3 Back diffused collector is 400-800 ohm/square.

2.4 N+ buried layer is selective in N islands only, 10-30 ohms/square.

2.5 N base is 130-160 ohm/square.

2.6 P base is 120-145 ohm/square.

2.7 P+ emitter is 14-18 ohm/square.

2.8 N+ emitter is 3.5-4.5 ohm/square.

2.9 Capacitor oxide over P+ is 2000Å for specific capacitance of 1.705×10^{-4} pF/μ^2.

2.10 Aluminum is 12,500Å.

2.11 Silox passivation 1000Å/6000Å/1000Å.

2.12 I^2 resistor. 250 ohms/square.

3.0 SCRIBE LINE RULES

3.1	Scribe centerline to inside scribe edge, all levels except silox.	75
3.2	Scribe centerline to inside scribe edge, silox level only.	50
3.3	Scribe overlap.	.5 mils
3.4	Bond pad to inside scribe edge, all levels except silox.	50
3.5	Silox bond pad to inside scribe edge, silox level only.	75
3.6	Inside scribe edge to active junction.	50
3.7	Any metal to scribe edge.	45

4.0 TRANSISTOR RULES

NOTE: Transistor rules apply to NPN and PNP devices.

4.1	Contact width.	5
4.2	Contact size.	7 X 5
4.3	Contact to edge of collector diffusion	5

4.4	Emitter contact to edge of emitter.	5
4.5	Emitter to base edge.	7
4.6	Emitter to base contact diffusion.	10
4.7	Base contact to edge of base contact diffusion.	5, 3 sides; 2, side facing emitter
4.8	Base to collector diffusion.	13, high breakdown device 5, low breakdown device
4.9	Interconnect width.	7
4.10	Interconnect spacing.	7
4.11	Interconnect overlap of contacts.	3
5.0	IMPLANTED RESISTOR RULES	
5.1	Minimum Resistor Width	13
5.2	Resistors are 250 ± 10% ohms/square for W = 13μ.	
5.3	All resistors have P+ end caps.	
5.4	Resistor Contact Aperture.	7 X 13
5.5	Contact to edge of P+.	5
5.6	Aperture is line-on-line with resistor end.	
5.7	No metal can cross I^2 resistor.	
5.8	Crossunders according to rules 5.9 and 5.11.	
5.9	Resistor overlap of P+.	8
5.10	Oversize I^2 mask is 5μ oversize of I^2 resistor.	
5.11	Resistor to edge of P+, on sides.	5
6.0	CAPACITOR RULES	
6.1	Metal overlap of thin oxide aperture.	3
6.2	Contact to edge of P+ diffusion.	5
6.3	Minimum island to P+ diffusion.	5
6.4	Thin oxide aperture to P+ edge.	5

7.0 BOND PAD RULES

7.1	Bond pad size.	110X110
7.2	Silox opening.	100X100
7.3	Silox opening spacing.	75
7.4	Silox opening to adjacent metal.	40
7.5	All bond pads have fillet of 20 X 50.	
7.6	Pad 1 uses distinctive shape.	
7.7	Minimum island to metal bond pad.	10

8.0 MISCELLANEOUS RULES

8.1 Alignment sequence

P Collector to flat
N+ buried layer to p collector
Isolation to P collector
N base to isolation
P base to N base
P+ to N base
N+ to N base
Capacitors to N base

I^2 resistors to N base

Oversize I^2 resistors to I^2 resistors.
Contacts to N base
Interconnect to contacts
Silox to interconnect
Oversize silox to silox

8.2 All masks are direct-stepped borosilicate hard-surface; alignment tolerance is .75μ except for silox which is 1μ.

8.3 All alignments are by cross into previously created box.

8.4 Front-to-back alignment is by cross-hair structure or by N base ring into depth indicator island.

8.5 Die has Harris Logo, year, copyright, 2nd mask number in metal level.

8.6 Die has large NPN and PNP device for in-line probing.

8.7 All critical PNP devices (insofar as collector base leakage is concerned) to have full collector guard ring of minimum 8 μ width.

Test Devices

Test and piloting devices include:

1. Grinding depth indicator for use during the polishing operation at the end of materials (backside) fabrication.

2. Large aperture NPN and PNP special geometry devices provided for probe and piloting steps prior to metallization.

3. PNP and NPN standard geometry test devices brought out to octagonal pads for final probe or hardness assurance tests.

4. SEM mark (crossed H) to check step coverage of aluminum.

5. Additional devices brought out individually on 5 test patterns (expanders) per slice, to be used for testing particular devices of interest.

PHOTODIODE DESIGN # 1

STEPPED D.I.

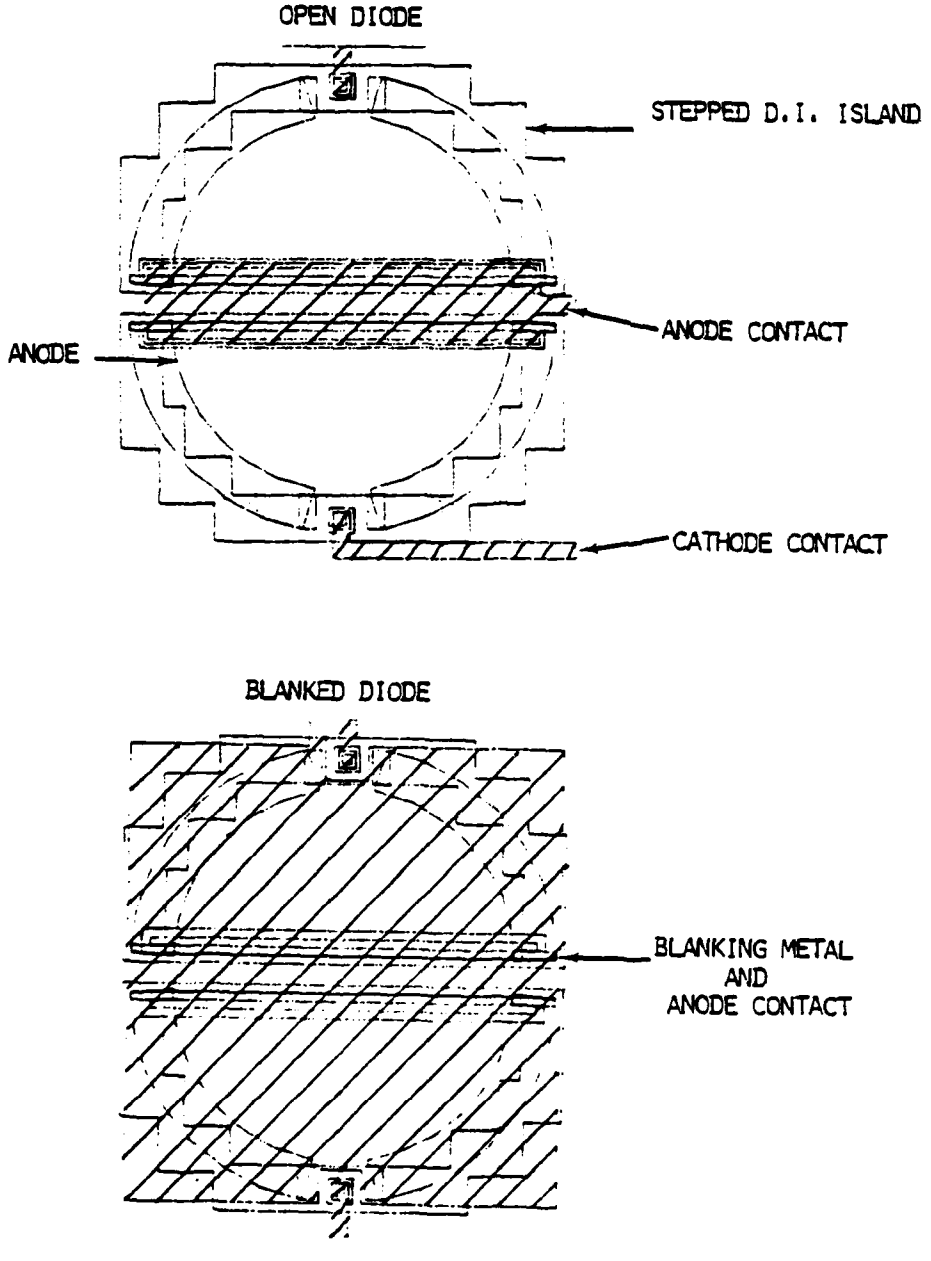


Figure 5.1.1

PHOTODIODE DESIGN #2

STEPPED D.I. & N+ RING

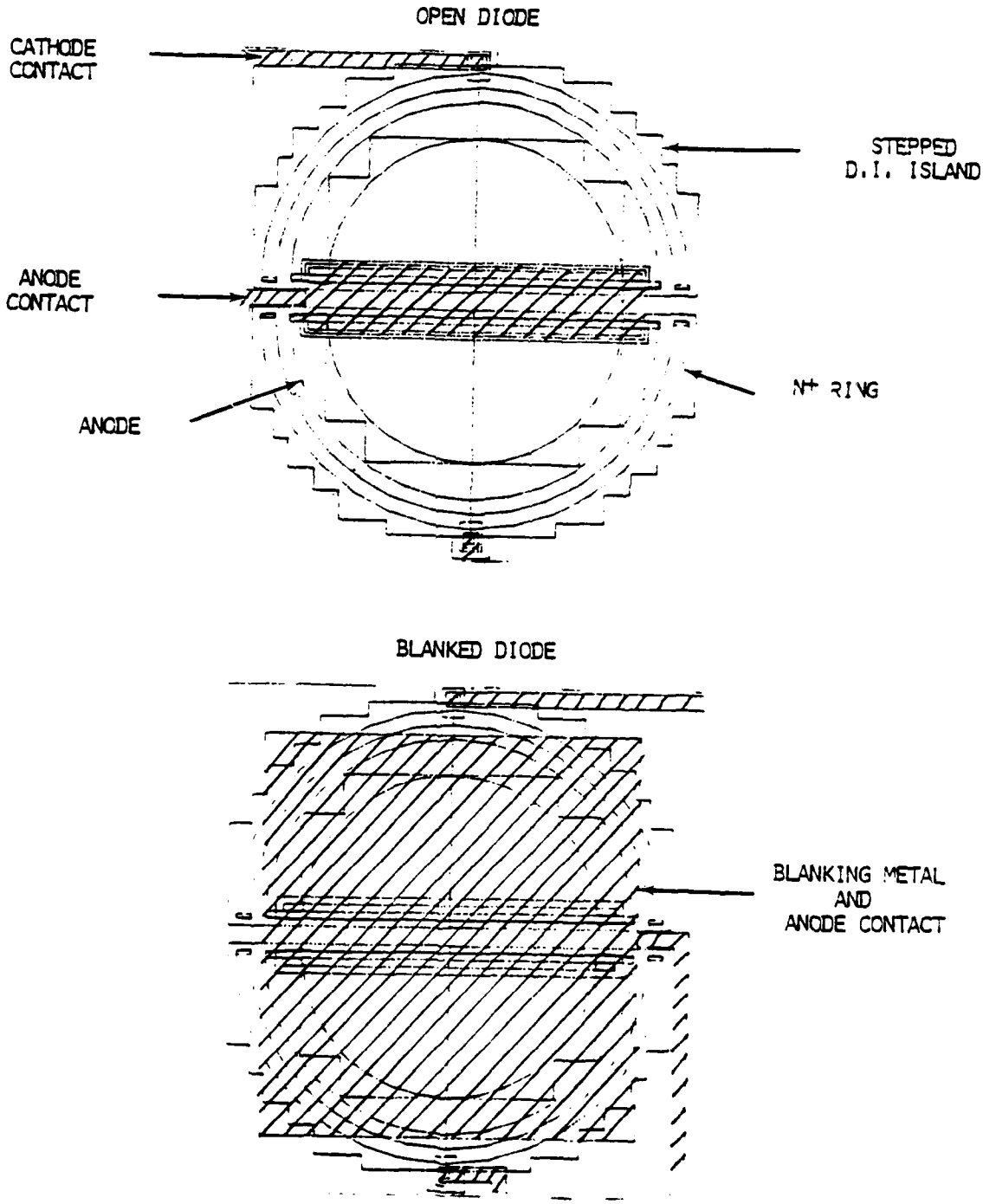


Figure 5.1.2

PHOTODIODE DESIGN #3

CIRCULAR D.I. ISLAND

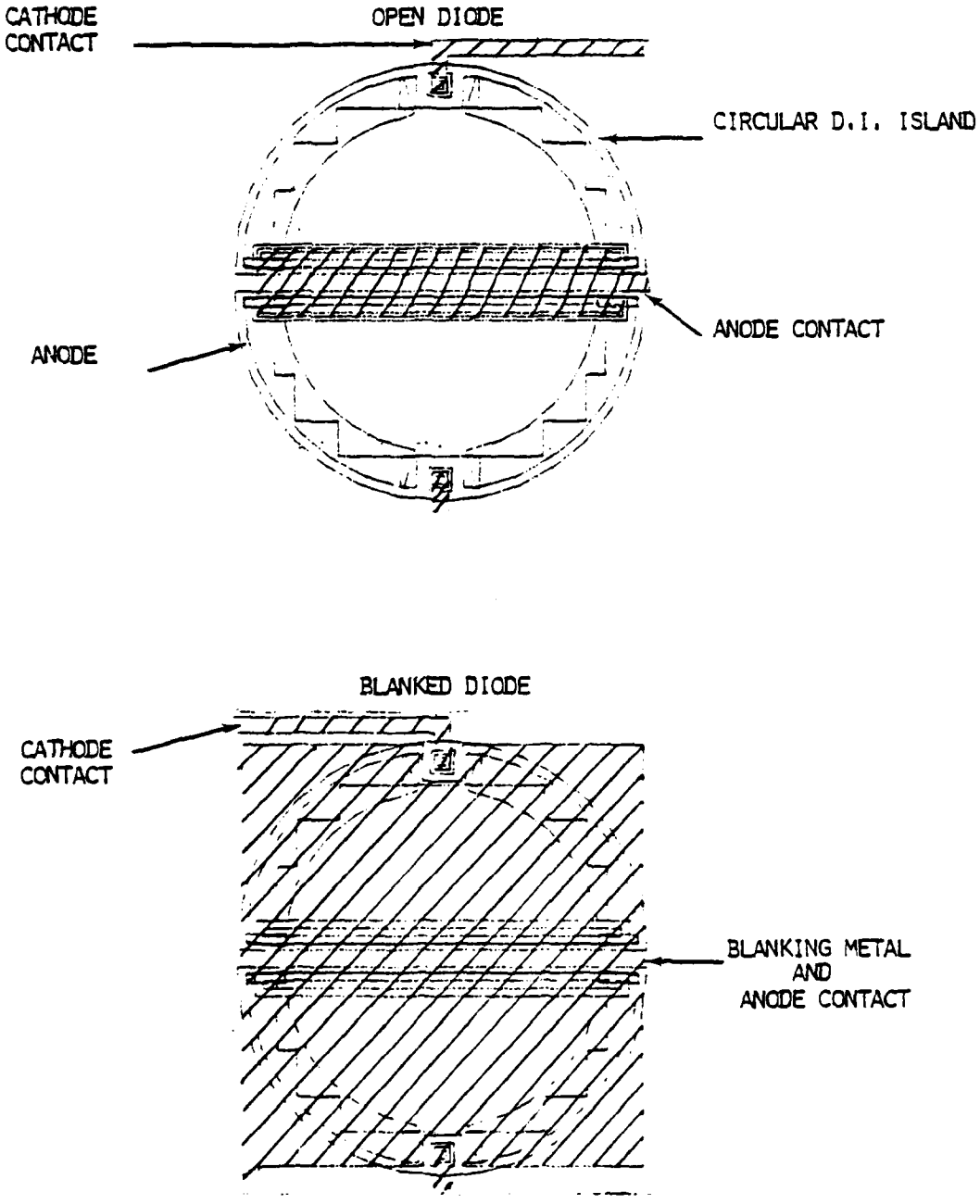


Figure 5.1.3

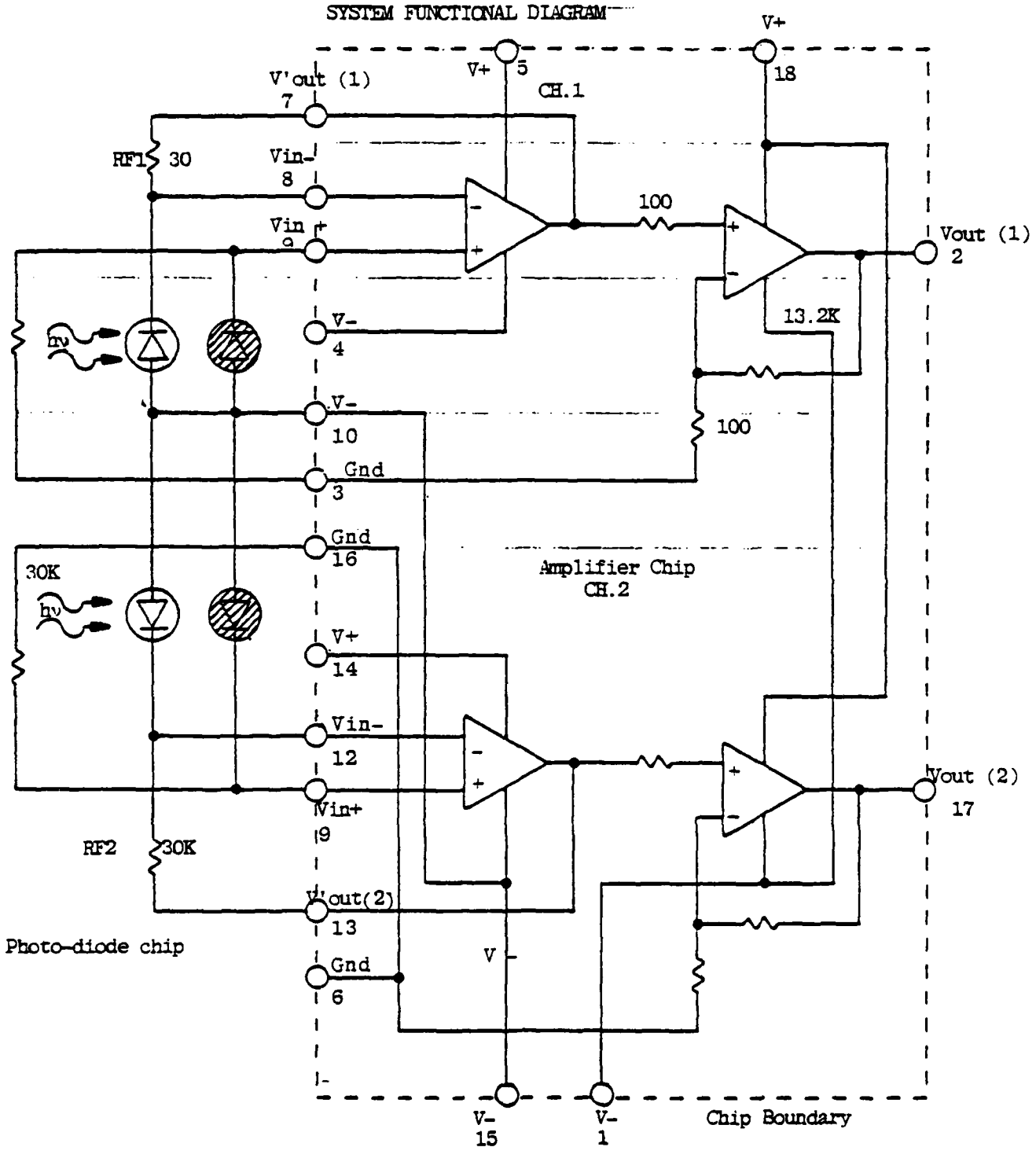
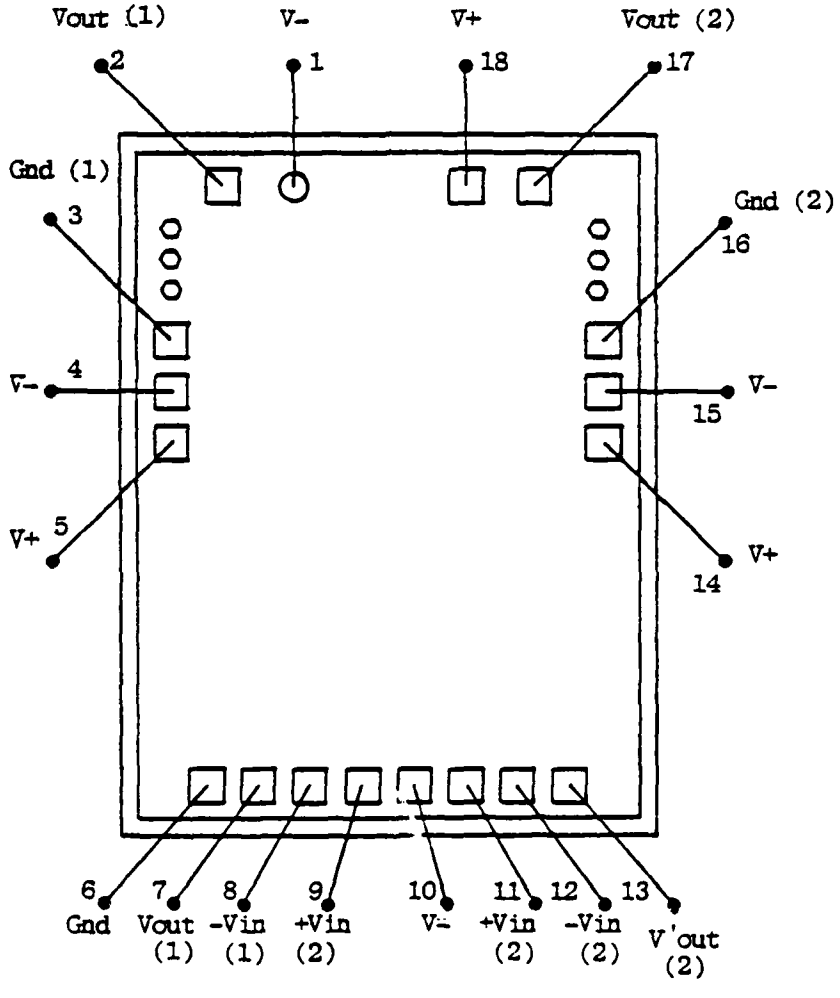

SYSTEM FUNCTIONAL DIAGRAM
V+
V+ 5
18
CH.1
V'out (1)
7
RF1 30
Vin-
8
Vin+
9
100
Vout (1)
2
13.2K
hν
V-
4
V-
10
100
Gnd
3
Gnd
16
30K
Amplifier Chip
CH.2
V+
14
Vin-
12
Vin+
9
Vout (2)
17
RF2
30K
V'out(2)
13
Photo-diode chip
Gnd
6
V-
V-
15
V-
1
Chip Boundary

FIGURE 5.1.4



DINS 1058

BONDING DIAGRAM

FIGURE 5.1.5

6.0 CHARACTERIZATION RESULTS

Electrical bench testing of the first pilot run of 1058 DINS Pre-amp IC's showed excellent results. All electrical requirements were achieved with good correlation to design simulations.

A summary specification sheet showing the parameters tested and the values measured is shown in Table 6.1. Six IC's from 2 wafers were used as test vehicles for characterization. Both wafers were from the same pilot run. The test chips were encapsulated in a 16 lead side brazed dip package. The test circuit diagram is shown in Figure 6.2.

Of particular concern, was the output response time and overshoot from an input current step. Figures 6.3 through 6.5 are photographs displaying the rise time and overshoot from one channel of a typical device at temperatures of -55°C, 25°, and +125°C respectively. The rise time and overshoot was measured with an input current step of 2.5 microamps.

Crosstalk isolation on all devices measured was approximately -58 db at 1.8 MHz. This high isolation was possible by separating the ground for each channel and providing each amplifier with separate VCC and VEE connections.

All devices exhibited a thermal R.M.S. output noise voltage of 14 mV. This noise component is insignificant when superimposed with the differential noise current generated by the DINS photodiodes due to prompt gamma radiation. This differential radiation photocurrent is due to finite volume mismatches between each common pair of photodiodes. Theoretical radiation noise current calculations and CAD simulations on output noise with different percentage photodiode volume mismatches are shown in the DINS design report. Figure 6.6 is a photograph of the DINS photodiodes and pre-amplifier wire bonded together. Note that the diodes are supplied with their own VEE bonding pad.

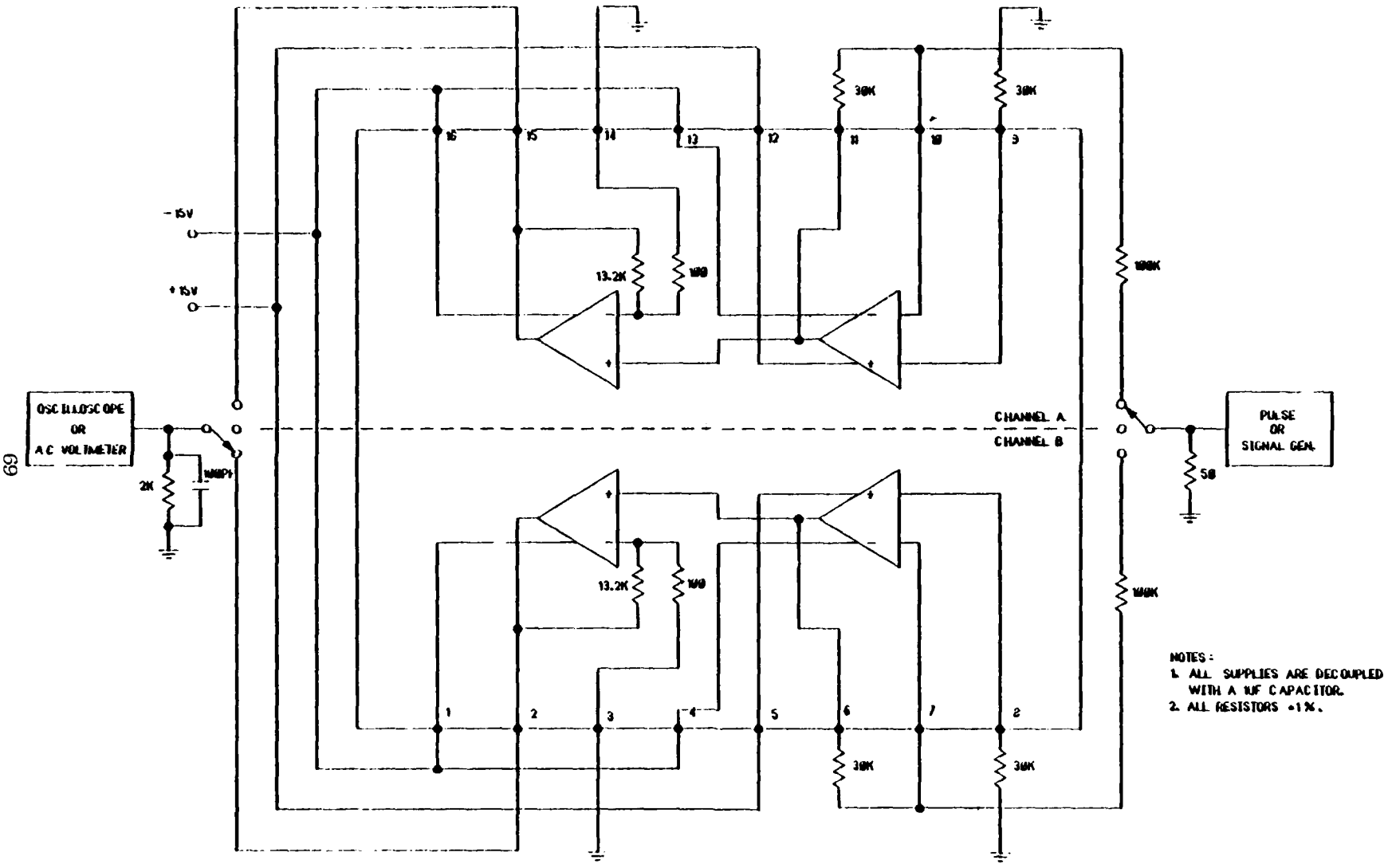
On all devices tested, channel to channel phase tracking was excellent. At 1.8 Mhz, the worst case measured value was +3° (channel A relative to B). Some of this error was possibly due to extrapolation since the scale on the HP-8047 was set at 10°/cm. Nevertheless, this deviation is well below the specified maximum channel to channel phase difference of ±15°.

Characterization of the DINS photodiode has been completed by MRC Inc. A summary of the results, including theoretical analysis and experimental comparisons is shown in the report titled; characterization of the Radiation Hard Harris/DINS Ring Laser Gyro Photodetectors; Contract #DNA-80-C-0140. Results indicate a photodiode responsivity of .4±.1 amperes/watt which is in close agreement with theoretical calculations.

TABLE 6.1

ELECTRICAL TEST DATA (DINS 1068 PRE-AMP)

SYMBOL.		ICC(mA)	IEE(mA)	VOS (VOLTS)	$\frac{Vo}{IIN}$ (MΩ)	B.W.(MHz)	%O.S.	t_r(ns)	tf(ns)	TEMP. °C
PARAMETER		POS. SUPPLY CURRENT	NEG. SUPPLY CURRENT	OUTPUT OFFSET VOLTAGE	LOW FREQ. GAIN	SMALL SIGNAL BANDWIDTH	% TRANSIENT OVERSHOOT	10-90% RISE TIME	10-90% FALL TIME	
UNIT #1	CH.A	6.9	8.7	-0.20	4.48	1.85	8.0	180	180	+25
	CH.B	6.9	8.7	-0.25	4.72	1.85	8.0	180	180	
UNIT #2	CH.A	7.1	8.7	+0.50	4.16	1.85	8.5	177	180	+25
	CH.B	7.1	8.7	+0.38	4.16	1.85	8.5	177	180	
UNIT #3	CH.A.	7.2	8.6	+0.60	4.22	1.73	7.0	185	187	+25
	CH.B	7.2	8.6	+0.44	4.22	1.73	7.0	185	187	
UNIT #3	CH.A	6.7	8.2	+0.15	4.27	1.86	6.0	180	180	-55
	CH.B	6.7	8.2	+0.10	4.27	1.86	6.0	180	180	
UNIT #3	CH.A	7.2	8.7	+0.70	4.37	1.78	12.5	175	175	+125
	CH.B	7.2	8.7	+0.50	4.37	1.78	12.5	175	175	
UNIT #4	CH.A	7.4	8.8	+0.28	3.96	1.85	8.5	190	190	+25
	CH.B	7.4	8.8	-0.03	4.20	1.80	8.5	190	190	
UNIT #5	CH.A	7.4	8.8	+0.45	3.48	1.80	8.0	178	180	-55
	CH.B	7.4	8.8	+0.37	3.56	1.85	8.0	178	180	
UNIT #6	CH.A	7.3	8.7	+0.78	3.64	1.85	8.5	178	182	+125
	CH.B	7.3	8.7	+0.02	3.76	1.85	8.5	178	182	



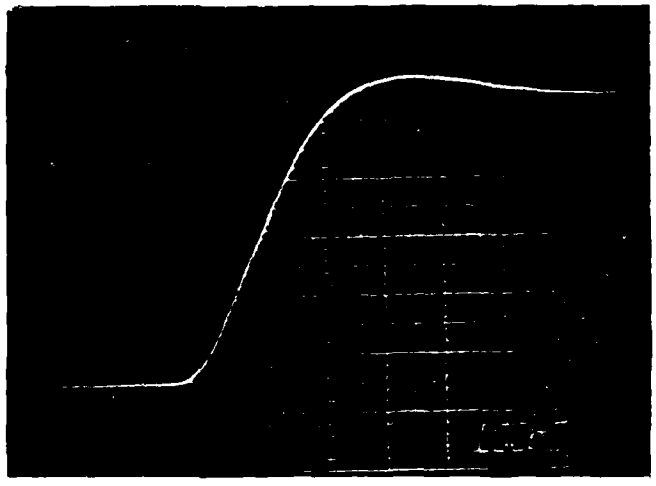
DINS TEST CIRCUIT DIAGRAM

FIGURE 6.2

OUTPUT TIME RESPONSE TO A
2.5 μA INPUT CURRENT STEP

+25°C

DEVICE #3
2 V/DIV.

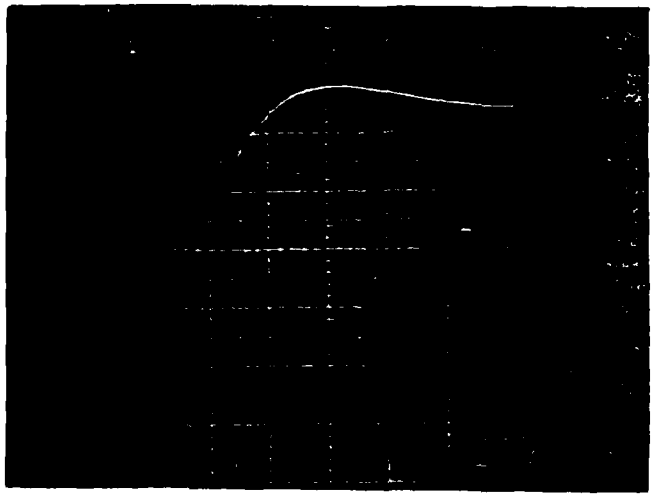


100 ns/DIV
TEMP. = +25°C

FIGURE 6.3

-55°C

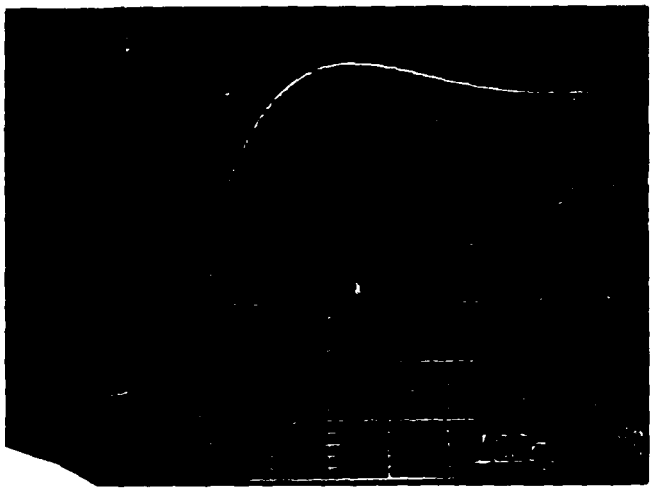
DEVICE #3
2 V/DIV.



100 ns/DIV.
TEMP. = -55°C

FIGURE 6.4

+125°C



DEVICE #3

2V/DIV.

100 ns/DIV.

TEMP. = +125°C

FIGURE 6.5

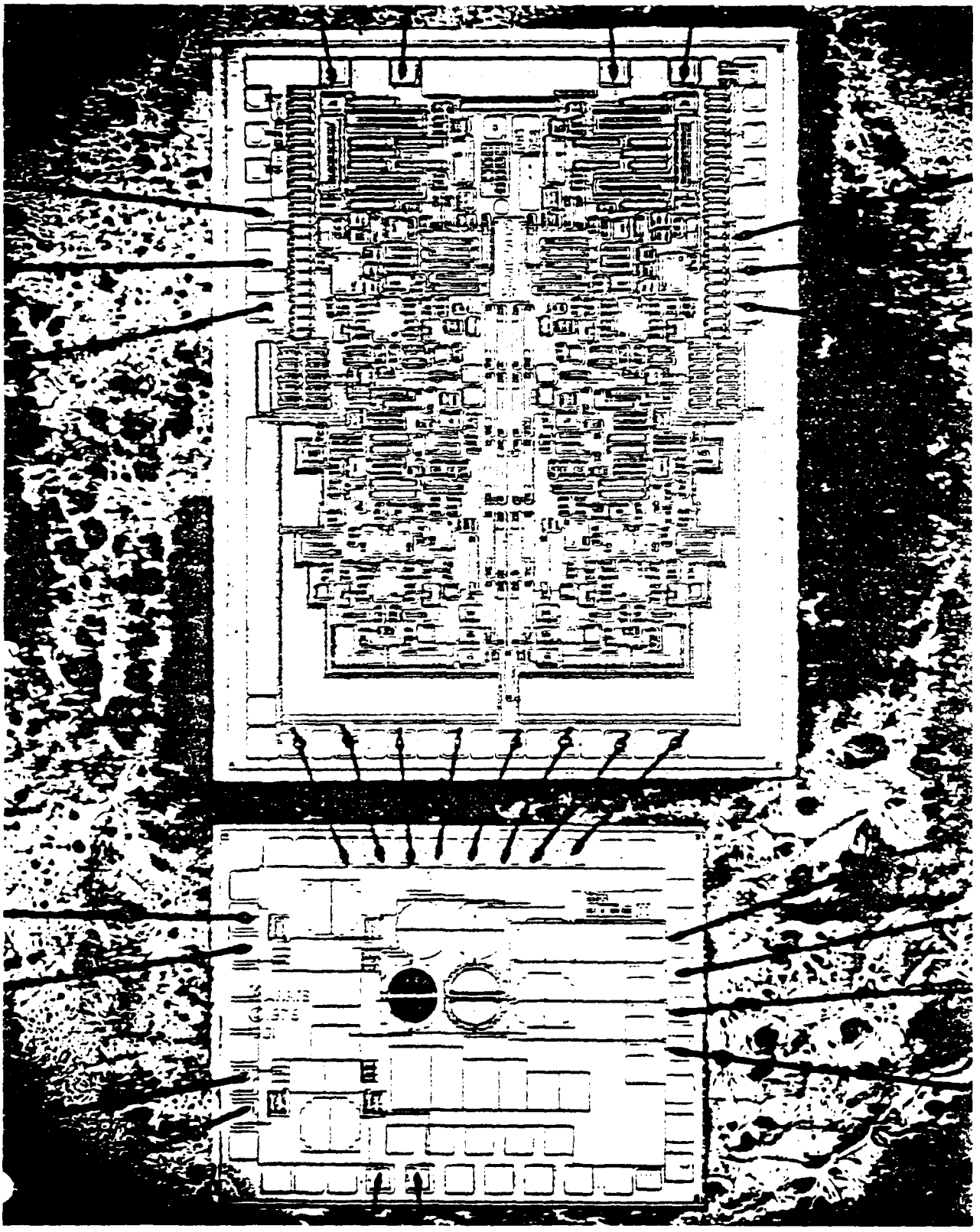


FIGURE 6.6

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